YSM146A

Data Sheet

8 Bit General Purpose OTP MCU

46-I/O with A/D, D/A, SPI, UART

Preliminary

Revision History

1.00	Initial Version
1.11	Preliminary Version
1.12	Add DC characteristic
1.13	DC Characteristic Modify

1.0 Device Overview

1.1 General Description:

The YSM146A is a 46 I/O PIN OTP-Base 8-bit microcontroller that is high performance, low cost RISC-MCU.

The YSM146A device has five-level deep stack, and external interrupt sources.

The YSM146A is a 16-bit wide instruction word, support the direct and indirect addressing mode.

There are four oscillator options, High Speed frequency crystal mode, Low-Speed frequency crystal mode, External Resistor/Capacitor oscillator mode and Internal Resistor/Capacitor mode.

The sleep mode offers power saving , user can wake-up YSM146A from sleep through external , internal and Reset.

1.2 Features:

- Only 50 instructions to learn.
- All instructions are single cycle except for program branches which are two cycle.
- 16-bit wide instruction.
- 8-level deep hardware stack.
- 4K x 16-bit OTP-ROM Program Memory.
- 256 x 8-bit RAM Data Memory.
- 46 General Purpose I/O PIN.
- Built-in Internal RC oscillator.
- Two system clocks per instruction cycle.
- 12 I/O Wake up PIN.
- 8-bit real time clock/counter
- 2 Open-Drain PIN can be defined.
- 2 Channel 8 bit resolution PWM (Pulse Width Modulation) Output.
- 16 Channel 10 bits resolution ADC
- 1 Channel 8 bits resolution DAC.
- 2 Sets SPI Port/ 1 Set PS2 Port/ 1 Set UART Port.
- 4 Type Hardware Interrupt:
  External / Timer0/ Timer1/ SPI Interrupt.
- Power On Reset

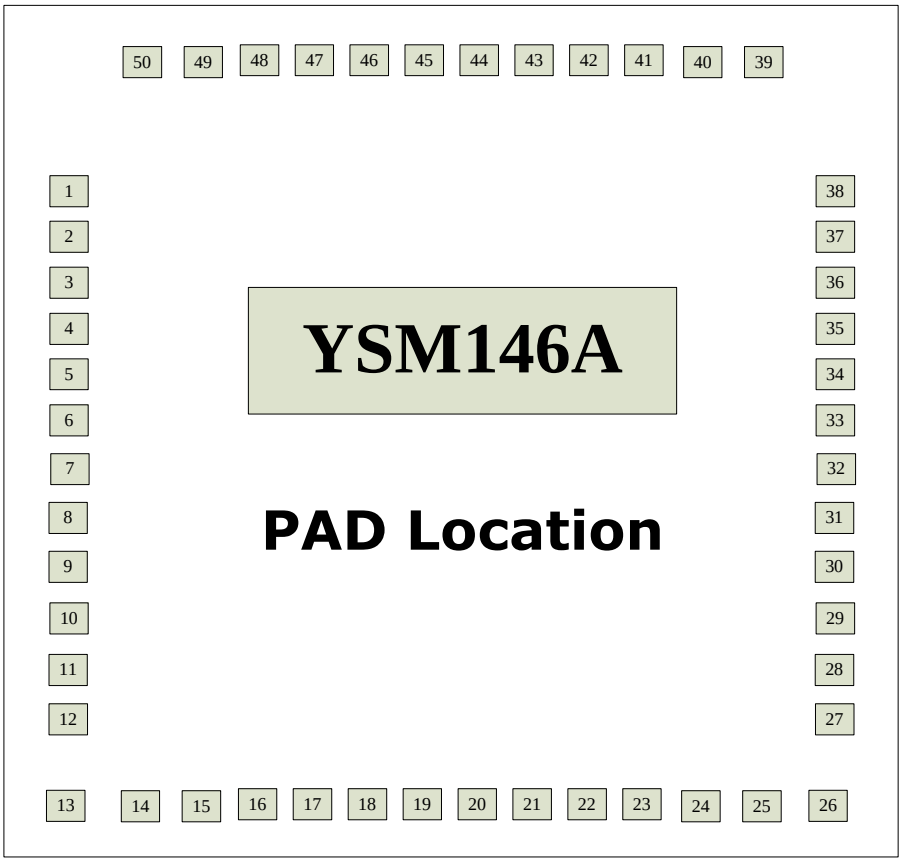
1.3 Pin Description

Pin Name	Pad Number	Type	Description
VDD	40	P	Power PAD, Positive Supply
VDDL	41	P	(a) System Power < 3.6V Connected with VDD. (b) System Power > 3.6V Connected with 0.1uF capacitor to VSS
VSS	17 44	P	Ground PAD
RESTN/PF5	39	I I/O	(a) Reset Pin, Low Active with pull-up. (b) PF3: Bi-direction I/O with pull-up and SMIT Input. ***Note: RESTN/PF5 by Code-Option.***
EINT/PF3	37	I I/O	(a) EINT : Interrupt PIN (b) PF3: Bi-direction I/O with pull-up and SMIT Input. ***Note: EINT/PF3 by Code-Option.***
OSCI/PF6	42	I I	(a) OSCI: Xtal Mode (Oscillator Crystal Iutput) RC Mode (Connected a resistor to VDD) (b) PF6: Input Port. ***Note: OSCI/PF6 by Code-Option.***
OSCO/PF7	43	O I	(a) OSCO: Xtal Mode (Oscillator Crystal output) RC Mode (Output internal system clock) (b) PF7: Input Port. ***Note: OSCO/PF7 by Code-Option.***
PA0/AD0 PA1/AD1 PA2/AD2 PA3/AD3 PA4/AD4 PA5/AD5 PA6/AD6 PA7/AD7	3 4 5 6 7 8 9 10	I/O	(a) Bi-direction I/O with pull-up selection by Program (b) When ADC Enable : PA0~PA7=AD0~AD7

PB0 PB1 PB2/SDI2 PB3/SDO2 PB4/SCK2 PB5/SS2 PB6/TX PB7/RX	18 19 20 21 22 23 24 25	I/O	(a) Bi-direction I/O with pull-up selection by Program, and it can be Wake-up by PIN Change. (b) When SPI2 Enable : PB2=SDI2, PB3=SDO2, PB4=SCK2 PB5=SS2; When UART Enable : PB6=TX, PB7=RX;
PC0/VREF PC1 PC2 PC3 PC4/CLK PC5/DATA	11 12 13 14 15 16	I/O	(a) PC0~PC3 : Bi-direction I/O Port. PC4~PC5 : Bi-direction I/O with pull-up. (b) When PS2 Mode : PC4=CLK, PC5=DATA; (c) When ADC VREF Enable : PC0=VREF.
PD0/AD8 PD1/AD9 PD2/AD10 PD3/AD11 PD4/AD12 PD5/AD13 PD6/AD14 PD7/AD15	45 46 47 48 49 50 1 2	I/O	(a) Bi-direction I/O with pull-up selection by Program (b) When ADC Enable : PD0~PD7=AD8~AD15 **(c) When DAC Enable :** **PD6 = DAC Output**
PE0/PWM1 PE1/PWM2	26 27		(a) Bi-direction I/O with pull-up selection by Program, and it can be Wake-up by PIN Change (b) PWM1~2 : PWM Output PIN
PE2/SDI1	28		(a) Bi-direction I/O with pull-up selection by Program (b) When SPI Enabled, as Serial Data IN PIN
PE3/SDO1	29		(a) Bi-direction I/O with pull-up selection by Program (b) When SPI Enabled, as Serial Data Out PIN
PE4/SCK1	30		(a) Bi-direction I/O with pull-up selection by Program (b) When SPI Enabled, as Serial Clock IN PIN

PE5/SS1	31		(a) Bi-direction I/O with pull-up selection by Program (b) When SPI Enabled, as Slave Selected PIN
PE6 PE7	32 33		Bi-direction I/O with pull-up selection by Program
PF0 PF1 PF2	34 35 36		Bi-direction I/O with pull-down and SMIT Input.
PF4/VPP	38		(a)Bi-direction open-drain I/O with pull-up and SMIT Input. (b)When OTP Programming, this is high voltage PIN.

1.4 Pad Location :



NO.	PAD NAME	X	Y	NO.	PAD NAME	X	Y
1	PD6/AD14/DAC	-649	447	15	PC4	-405	-704
2	PD7/AD15	-649	357	16	PC5	-315	-704
3	PA0/AD0	-649	267	17	VSS	-225	-704
4	PA1/AD1	-649	177	18	PB0	-135	-704
5	PA2/AD2	-649	87	19	PB1	-45	-704
6	PA3/AD3	-649	-3	20	PB2/SDI2	45	-704
7	PA4/AD4	-649	-93	21	PB3/SDO2	135	-704
8	PA5/AD5	-649	-183	22	PB4/SCK2	225	-704
9	PA6/AD6	-649	-273	23	PB5/SS2	315	-704
10	PA7/AD7	-649	-363	24	PB6/TX	405	-704
11	PC0/VREF	-649	-453	25	PB7/RX	495	-704
12	PC1	-649	-543	26	PE0/PWM1	645	-704
13	PC2	-645	-704	27	PE1/PWM2	649	-543
14	PC3	-495	-704	28	PE2/SDI1	649	-453

NO.	PAD NAME	X	Y		NO.	PAD NAME	X	Y
29	PE3/SDO1	649	-363		40	VDD	405	704
30	PE4/SCK1	649	-273		41	VDDL	315	704
31	PE5/SS1	649	-183		42	OSCI/PF6	225	704
32	PE6	649	-93		43	OSCO/PF7	135	704
33	PE7	649	-3		44	VSS	45	704
34	PF0	649	87		45	PD0/AD8	-45	704
35	PF1	649	177		46	PD1/AD9	-135	704
36	PF2	649	267		47	PD2/AD10	-225	704
37	EINT/PF3	649	357		48	PD3/AD11	-315	704
38	PF4/VPP	649	447		49	PD4/AD12	-405	704
39	RSTN/PF5	495	704		50	PD5/AD13	-495	704

Table of Contents

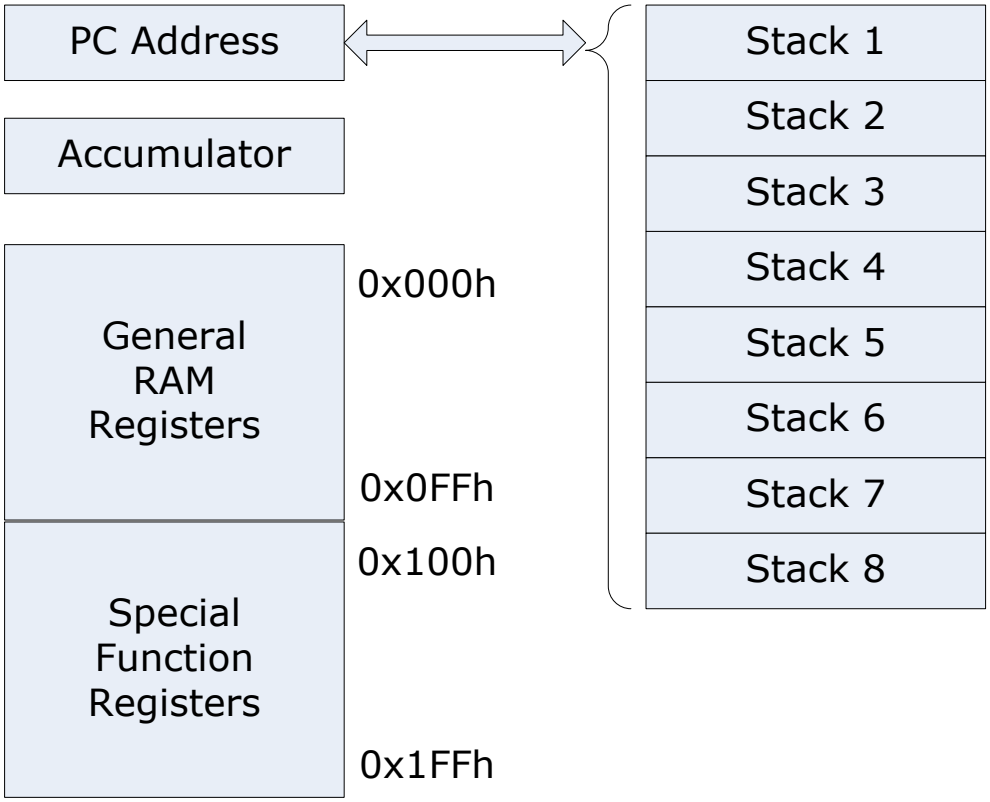
2.0 Memory Organization

2.1 ROM Structure

Address	***Description***
0x0000	**Program Area** General coding area.
0x0001	**Hardware Interrupt Vector** (Timer0,Timer1,SPI,External Interrupt)
0x0002	**Software Interrupt Vector** When do the INT Instruction.
0x0003 ~ 0x0FFE	**Program Area** General coding area.
0x0FFF	**Reset Vector** Power-On , RSTN PIN go low.

Address	***Description***
N/A	**Option Codes** The ROM space which used to store the device options.

2.2 RAM Structure



There are 256 bytes general purpose registers(GPRs) in RAM of the MCU, User can use these GPRs by direct addressing without any page/bank change commands.

The 2nd block of the RAM space are the Special Function Registers(SFRs). These are being accessed like GPRs by direct addressing.

Notes. GPRs/SFRs can only move the value to/from the accumulator.

2.3 RAM – Special Function Registers(SFRs) Overview

YSM146 Special Function Registers									
NAME	**ADDR**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
INDR	0x100	**Indirect Addressing Register**							
TMR0	0x101	**8 bit Real Time Clock / Counter**							
PCL	0x102	**Low 8 bits Program Counter Register**							
STATUS	0x103	GPR	-	-	/TO	/PD	Z	DC	C
RAMS	0x104	**Indirect Data Memory Address Point**							
PORTA	0x105	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PORTB	0x106	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
PORTC	0x107	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
PORTD	0x108	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
PORTE	0x109	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PW0
MCRW	0x122	/PUE	GIE	-	-	PAB	PS2	PS1	PS0
MCRR	0x124	/PUE	GIE	-	-	PAB	PS2	PS1	PS0
IORA	0x125	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
IORB	0x126	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
IORC	0x127	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
IORD	0x128	IOD7	IOD6	IOD5	IOD4	IOD3	IOD2	IOD1	IOD0
IORE	0x129	IOE7	IOE6	IOE5	IOE4	IOE3	IOE2	IOE1	IOE0
T1CON	0x12C	-	-	-	-	-	TR1S	TR1P1	TR1P0
IOPH	0x12D	SSPC	-	-	/PUC	/PUE	/PUD	/PUB	/PUA
WDTS	0x12E	-	ODE	WDTE	SLP2E	-	-	-	/WUE
INTE	0x12F	-	-	-	-	TR1IE	SPIIE	EXIE	TR0IE
PWM1D	0x130	**PWM1 Duty Cycle Data Register**							
PWM2D	0x131	**PWM2 Duty Cycle Data Register**							
PWM1P	0x132	**PWM1 Period Data Register**							
PWM2P	0X133	**PWM2 Period Data Register**							
PWMC	0x134	PW2E	PW1E	-	-	-	PWS2	PWS1	PWS0
SPIRB	0x13A	**SPI Data Read Buffer**							
SPIWB	0x13B	**SPI Data Write Buffer**							
SPIS	0x13C	**SPI Status Register**							
SPIC	0x13D	CES	SPIE	SRO	SSE	-	SBRS2	SBRS1	SBRS0

YSM146 Special Function Registers(Continue)									
NAME	**ADDR**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
TMR1	0x13E	**Timer1 Value Register**							
TR1CV	0x13F	**Timer 1 Comparator Value Register**							
ADCON1	0X140	ADC	ADEN	ACHEN		CHS3	CHS2	CHS1	CHS0
ADLSB	0X141	AD01	AD00	-	-	-	-	-	-
ADMSB	0X142	AD09	AD08	AD07	AD06	AD05	AD04	AD03	AD02
ADCON2	0X143	VREFS					ADCS2	ADCS1	ADCS0
PORTF	0X148	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
IORF	0X149	IOF7	IOF6	IOF5	IOF4	IOF3	IOF2	IOF1	IOF0
PAL	0x14B	**Low- Byte Address of Data Latch**							
PAH	0x14C	**High-Byte Address of Data Latch**							
DACR	0x14D	DAEN	-	CVC2	CVC1	CVC0	-	-	-
DADAT	0x14E	**DAC Data Register**							
UCON	0x150	UAEN	RXEN	RXIE	-	BAUDS	TXSF	RXSF	RXOF
UBAUD	0x151	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0
UBUF	0x152	UBUF7	UBUF6	UBUF5	UBUF4	UBUF3	UBUF2	UBUF1	UBUF0
SPIRB2	0x15A	**SPI2 Data Read Buffer**							
SPIWB2	0x15B	**SPI2 Data Write Buffer**							
SPIS2	0x15C	**SPI2 Status Register**							
SPIC2	0x15D	CES	SPIE	SRO	SSE	ORD	SBRS2	SBRS1	SBRS0
INTF	0x17F	-	-	-	-	TR1IF	SPIIF	EXIF	TR0IF

2.4 Special Function Registers(SFRs) Briefing

◆ **INDR** (0x100) : ***Indirect Addressing Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INDR	Indirect Addressing Register							
R/W	R/W							
RESET	-	-	-	-	-	-	-	-

The INDR Register is not a physical register. Addressing INDR actually address the register that RAMS address value. User should use SFR:INDR with SFR:RAMS to access the indirect addressing data.
See : Page 15

◆ **TMR0** (0x101) : ***8Bits Real Timer Clock/Counter***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMR0	8 bit Real Time Clock / Counter							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

The TMR0 special function register is the clock counter value which the clock source is from an 8bits real time clock. And the clock source of the 8bits real time clock is from the instruction cycle(Fosc / 2).

◆ **PCL** (0x102) : ***Program Counter Lower 8 bits data***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMR0	Low 8 bits Program Counter Register							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

The PCL special function register is the lower 8 bits data of the program counter.

◆ **STATUS** (0x103) : ***Status Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STATUS	GPR	-	-	/TO	/PD	Z	DC	C
R/W	R/W			R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	1	1	0	0	0

GPR : ***General Purpose Read/Write bit***

/TO : ***Time- Out Flag***

/TO=0 Watch dog Timer Overflow.

/TO=1 (a) Power On

(b) Execute WDTC or SLEEP Instruction.

/PD : ***Power Down Flag***

/PD=0 After SLEEP Instruction.

/PD=1 (a) Power On

(b) Execute WDTC Instruction.

Z : ***ALU Operation Zero Flag***

Z=0 Operation Result is not Zero.

Z=1 Operation Result is Zero.

DC : ***ALU Operation Half Carry /Borrow Flag***

DC=0 Half Carry/Borrow does not occur.

DC=1 Half Carry/Borrow occurred.

C : ***ALU Operation Carry /Borrow Flag***

C=0 Carry/Borrow does not occur.

C=1 Carry/Borrow occurred.

◆ **RAMS** (0x104) : ***Indirect Addressing Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RAMS	Indirect Data Memory Address Point							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

The RAMS register is a pointer for Indirect Addressing . User should use SFR:INDR with SFR:RAMS to access the indirect addressing data.
See : Page 15

◆ **PORTA** (0x105) : ***Port A Data***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PA0~PA7 : *I/O Port Read/Write Data*

◆ **PORTB** (0x106) : ***Port B Data***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PORTB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PB0~PB7 : *I/O Port Read/Write Data*

◆ **PORTC** (0x107) : ***Port C Data***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PORTC	-	-	PC5	PC4	PC3	PC2	PC1	PC0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
RESET	-	-	0	0	0	0	0	0

PC0~PC7 : *I/O Port Read/Write Data*

◆ **PORTD** (0x108) : ***Port D Data***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PORTD	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PD0~PD7 : *I/O Port Read/Write Data*

◆ **PORTE** (0x109) : ***Port E Data***

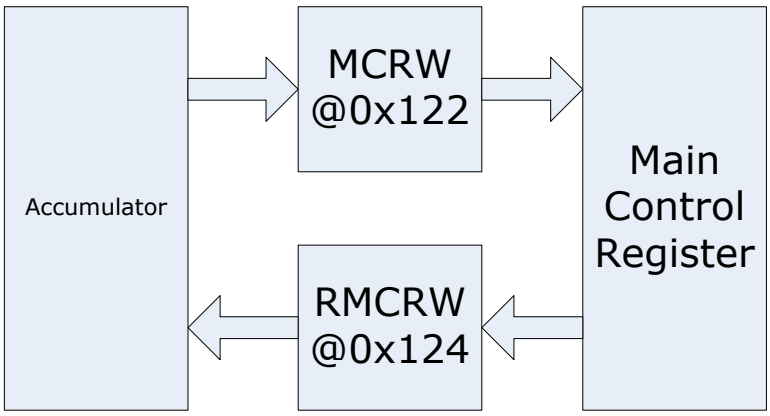
NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PORTE	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

PE0~PE5 : *I/O Port Read/Write Data*

◆ **MCRW** (0x122) : ***Main Control Register for Write***

◆ **MCRR** (0x124) : ***Main Control Register for Read***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCRR	/PUE	GIE	-	-	PAB	PS2	PS1	PS0
R/W	R/W	R/W			R/W	R/W	R/W	R/W
RESET								



(Continue)

/PUE : ***I/O Port Pull-Up Resistor Enable*** .

/PUE=0 : I/O Connected with Pull-Up Resistor.

/PUE=1 : Pull-Resistor Disconnected.

GIE : ***Global Interrupt Enable.***

GIE=0 Disable all interrupts. Execute DISI Instruction or accept Interrupt then GIE will be set to '0'. Reject any other Interrupt.

GIE=1 Global Enable all the Interrupt (Enable or not depend on others Register Enable Bit.
Execute ENI or RETI will be set to '1'. then accept others Interrupt.

PAB : ***Prescaler bit Assignment .***

PAB=0 Assign to TMR0 (Timer 0).

PAB=1 Assign to WDT (Watch-Dog Timer).

PS2~PS0 : ***Prescaler bits.***

PS2	PS1	PS0	TMR0 Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

◆ **IORA** (0x125) : ***Port A I/O Direction Setting***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IORA	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

◆ **IORB** (0x126) : ***Port B I/O Direction Setting***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IORB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

◆ **IORC** (0x127) : ***Port C I/O Direction Setting***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IORC	-	-	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
RESET	-	-	1	1	1	1	1	1

◆ **IORD** (0x128) : ***Port D I/O Direction Setting***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IORD	IOD7	IOD6	IOD5	IOD4	IOD3	IOD2	IOD1	IOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

◆ **IORE** (0x129) : ***Port E I/O Direction Setting***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IORE	IOE7	IOE6	IOE5	IED4	IOE3	IOE2	IOE1	IOE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

IOx0~IOx7 : *I/O as a Input or Output*

IOx0~7=0 , as a Output.

IOx0~7=1 , as a Input.

Port B can be Wake Up (from High to Low) after Sleep if (/WUE)=0.

◆ **T1CON** (0x12C) : ***Timer 1 Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
T1CON	-	-	-	-	-	TR1S	TR1P1	TR1P0
R/W						R/W	R/W	R/W
RESET								

TR1S : ***Timer 1 Turn On Bit***

TR1S=0 , Timer 1 turn off.

TR1S=1 , Timer 1 turn on.

TR1P1,TR1P0 : ***Timer 1 Prescaler Rate***

TR1P1	TR1P0	TMR0 Rate
0	0	1:1
0	1	1:4
1	0	1:8
1	1	1:16

◆ **IOPH** (0x12D) : ***I/O Port Pull High Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOPH	SSPC	-	-	/PUC	/PUE	/PUD	/PUB	/PUA
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W
RESET								

/PUA~E : ***Each I/O Port Pull-High Enable Bit***

/PUA~E=0 , Enable (Connected with pull high Resistor).

/PUA~E=1 , Disable.

◆ **WDTS** (0x12E) : ***Watch Dog & Wake Up Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WDTS	-	ODE	WDTE	SLP2E	-	-	-	/WUE
R/W	-	R/W	R/W	R/W	-	-	-	R/W
RESET								

ODE : ***Open Drain Control Bit for PC6 & PC7***

ODE=0 , PC6 & PC7 are Normal I/O Port.

ODE=1 , PC6 & PC7 are Open Drain Port.

/WUE : I/O Port PIN Wake Up Enable

/WUE=0 , Port B, Port C4,C5 & Port E can be wake –up

Wake Up Condition : As a Input Port & Input Signal from High to Low .

/WUE=1 , Disable PIN Wake Up Function.

I/O Port as a Wake Up PIN Setting Procedure:

Step 1: Setting as a Input PIN

Step 2: Pull High Enable .

Step 3: Enable Wake Up Function

Step 4: Enter to Sleep.

◆ **INTE** (0x12F) : ***Hardware Interrupt Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTE	-	-	-	-	TR1IE	SPIIE	EXIE	TR0IE
R/W					R/W	R/W	R/W	R/W
RESET					0	0	0	0

TR0IE : ***Timer 0 Interrupt Enable***

TR0IE=0 , Timer 0 Interrupt Disable .

TR0IE=1 , Timer 0 Interrupt Enable .

TR1IE : ***Timer 1 Interrupt Enable***

TR1IE=0 , Timer 1 Interrupt Disable .

TR1IE=1 , Timer 1 Interrupt Enable .

◆ **PWM1D** (0x130) : ***PWM1 Duty Cycle Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM1D	P1D7	P1D6	P1D5	P1D4	P1D3	P1D2	P1D1	P1D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

◆ **PWM2D** (0x131) : ***PWM2 Duty Cycle Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM2D	P2D7	P2D6	P2D5	P2D4	P2D3	P2D2	P2D1	P2D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P1D7~P1D0 : ***8 bits PWM1 Duty Cycle Data***

P2D7~P2D0 : ***8 bits PWM2 Duty Cycle Data***

◆ **PWM1P** (0x132) : ***PWM1 Period Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM1P	P1P7	P1P6	P1P5	P1P4	P1P3	P1P2	P1P1	P1P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

◆ **PWM2P** (0x133) : ***PWM2 Period Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM2P	P2P7	P2P6	P2P5	P2P4	P2P3	P2P2	P2P1	P2P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P1P7~P1P0 : ***8 bits PWM1 Period Data , PWM1 Signal Output from PE0 PIN.***

P2P7~P2P0 : ***8 bits PWM2 Period Data , PWM2 Signal Output from PE1 PIN.***

◆ **PWMC** (0x134) : ***PWM Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWMC	PW2E	PW1E	-	-	-	PWS2	PWS1	PWS1
R/W	R/W	R/W	-	-	-	R/W	R/W	R/W
RESET	0	0	-	-	-	0	0	0

PW2E : ***PWM2 Enable Bit***

PW2E=0 , PWM2 Disable.

PW2E=1 , PWM2 Enable.

PW1E : ***PW12 Enable Bit***

PW1E=0 , PWM1 Disable.

PW1E=1 , PWM1 Enable.

PWS2,PWS1,PWS0 : PWM Clock Prescaler *Rate*

PWS2	PWS1	PWS0	PWM Clock Rate
0	0	0	Fosc/2
0	0	1	Fosc/4
0	1	0	Fosc/8
0	1	1	Fosc/16
1	0	0	Fosc/32
1	0	1	Fosc/64
1	1	0	Fosc/128
1	1	1	Fosc/256

◆ **SPIRB**(0X13A) : ***SPI Data Read Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIRB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R/W-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

◆ **SPIWB**(0X13B) : ***SPI Data Write Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIWB	WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0
R/W-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

SPIRB Register is a 8 bits Data Buffer for SPI Data Read In.
SPIWB Register is a 8 bits Data Buffer for SPI Data Write Out.

◆ **SPIS**(0X13C) : ***SPI Status Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIS	-	-	-	-	ODO	ODC	RBFIF	RBF
R/W-	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

ODO : *SDO Open-Drain Control*

ODO=0 ,SDO Open-Drain Disable.
ODO=1 ,SDO Open-Drain Enable.

ODC : *SCK Open-Drain Control*

ODC=0 ,SCK Open-Drain Disable.
ODC=1 ,SCK Open-Drain Enable.

RBFIF : *SPI Read Buffer Full Interrupt Flag*

RBFIF=1 ,(a)Receive Completed, and Read Buffer is Full.
(b) Under the Interrupt Enable, and Interrupt Occur.
RBFIF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

RBFIF : *SPI Read Buffer Full Flag*

RBF=1 ,Receive Completed, and Read Buffer is Full.
RBF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

◆ **SPIC**(0X13D) : ***SPI Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIC	CES	SPIE	SRO	SSE	ORD	SBRS2	SBRS1	SBRS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	-	0	0	0	0

CES : *SPI Clock Edge Selection*

CES=0 , **Low go High** , Data Out; **High go Low** Data In.

CES=1 , **High go Low** , Data Out; **Low go High** Data In.

SPIE : *SPI Enable*

SPIE=0 ,SPI Disable.

SPIE=1 ,SPI Enable.

SRO : *Data In Overflow Flag (Only Used SLAVE Mode)*

SRO=1 ,Last Byte Data in SPI Read Buffer had not Read Out .

SRO=0 ,Otherwise.

SSE : *Start Shift SPI Data Out*

SSE=1 ,(a)Start Shift SPI Data Out.

(b) Completed Working , Clear SSE bit by Hardware .

SRO=0 ,Otherwise.

ORD : *SPI Data Shift Order*

ORD=0 ,MSB Bit First.

ORD=1 ,LSB Bit First.

SBRS2~SBRS0 : *SPI Baud Rate & Mode Selection*

SBRS~SBRS0 : ***Selection bits for Baud Rate & Mode***

SBRS	SBRS1	SBRS0	Mode	Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Slave	SS Enable
1	1	0	Slave	SS Disable
1	1	1	Master	TMR1/2

◆ **TMR1** (0x13E) : ***Timer 1 Value Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMR1	Timer 1 Value Register							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

◆ **TR1CV** (0x13F) : ***Timer 1 Comparator Value Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TR1CV	Timer 1 Comparator Value Register							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

◆ **ADCON1**(0X140) : ***A/D Control Register #1***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADCON1	ADC	ADEN	ACHEN	-	CHS3	CHS2	CHS1	CHS0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
RESET	0	0	0	-	0	0	0	0

ADC : ***ADC Start Transfer & Completed Flag***

ADC=0 , ADC is be Transfer Completed.(Clear by MCU Hardware)

ADC=1 , ADC Start Transfer.

ADEN : ***ADC Converter Enable***

ADEN=0 , ADC Converter Disable.

ADEN=1 , ADC Converter Enable.

ACHEN : ***ADC Converter Channel Enable***

ACHEN=0 , ADC Converter Channel Disable.

ACHEN=1 , ADC Converter Channel Enable.

CHS3~CHS0 : ***ADC Channel Selection***

CHS3~CHS0 = Channel 15~0.

◆ **ADLSB**(0X141) : ***A/D Digital Data LSB 2bits of 10bits***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADLSB	AD01	AD00	-	-	-	-	-	-
R/W	R/W	R/W	-	-	-	-	-	-
RESET	0	0	-	-	-	-	-	-

AD09~AD02 : ***ADC Transfer to Digital Data bit9~bit0***

◆ **ADMSB**(0X142) : ***A/D Digital Data MSB 8bits of 10bits***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADMSB	AD09	AD08	AD07	AD06	AD05	AD04	AD03	AD02
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

AD09~AD02 : ***ADC Transfer to Digital Data bit9~bit0***

◆ **ADCON2**(0X143) : ***A/D Control Register #2***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADCON2	VREFS	-	-	-	-	ADCS2	ADCS1	ADCS0
R/W	R/W	-	-	-	-	R/W	R/W	R/W
RESET	0	-	-	-	-	0	0	0

VREFS : ***ADC Power Source Selection***

VREFS=0 , ADC Power Source use Internal LDO Output.

VREFS=1 , ADC Power Source use External power from PAD **PC0**.

Note Input Power Voltage must be lower than 3.6V.

ADCS2~ADCS0 : ***ADC CLK Source:***

ADCS2	ADCS1	ADCS0	Clock (Hz)
0	0	0	Fosc/4
0	0	1	Fosc/8
0	1	0	Fosc/12
0	1	1	Fosc/16
1	0	0	Fosc/20
1	0	1	Fosc/24
1	1	0	Fosc/28
1	1	1	Fosc/32

◆ **PORTF** (0x148) : ***Port F Data***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PORTF	PF7	PF6	PF5	PF4	PE3	PE2	PE1	PE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

PF0~PF7 : *I/O Port Read/Write Data*

◆ **IORF** (0x149) : ***Port F I/O Direction Setting***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IORF	IOF7	IOF6	IOF5	IOF4	IOF3	IOF2	IOF1	IOF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

IOF0~IOF7 : *I/O as a Input or Output*

IOF0~7=0 , as a Output.

IOF0~7=1 , as a Input.

◆ **PAL** (0x14B) : ***Low Byte Address of The Data Latching***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PAL	Data Latching Address Low Byte Part							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

◆ **PAH** (0x14C) : ***High Byte Address of The Data Latching***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PAL	Data Latching Address High Byte Part							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

◆ **DACR** (0x14D) : ***DAC Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DACR	DAEN	-	CVC2	CVC1	CVC0	-	-	-
R/W	R/W	-	R/W	R/W	R/W	-	-	-
RESET	0	-	0	0	0	-	-	-

DAEN : ***DAC Enable Bit***

DAEN=0 , DAC Disable.

DAEN=1 , DAC Enable.

CVC2~CVC0 : Current Level Setting

CVC2~CVC0=0;0;0 , DAC current = Off.

CVC2~CVC0=1;0;0 , DAC current = 1X.

CVC2~CVC0=0;0;0 , DAC current = 2X.

◆ **DADAT** (0x14E) : ***DAC Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DADAT	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

DAC7~DAC0 : ***8 bits Digital Data***

Note: DAC Current Output from PC5 PIN

◆ **UCON**(0X150) : ***UART Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UCON	UAEN	RXEN	RXIE	-	BAUDS	TXSF	RXSF	RXOF
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
RESET	0	0	0	-	0	0	0	0

UCON : *UART Enable*

UCON=0 , UART Disable.

UCON=1 , UART Enable.

RXEN : *UART Reception Enable*

RXEN=0 , UART Reception Disable.

RXEN=1 , UART Reception Enable.

RXIE : *UART Interrupt Enable when data receive completed*

RXIE=0 , UART Interrupt Disable.

RXIE=1 , UART Interrupt Enable.

BAUDS : *Baud Rate CLK Selection*

BAUDS=0 , Baud Rate CLK = Fosc/4.

BAUDS=1 , Baud Rate CLK = Fosc/16.

TXSF : *UART Transmit Flag*

TXSF=1 , UART under transmitting state.

TXSF=0 , Otherwise.

RXSF : *UART Receive Flag*

RXSF=1 , UART under receiving state.

RXSF=0 , Otherwise.

RXOF : *UART Received Completed Flag*

RXOF=1 UART Received Completed , Set by MCU Hardware.

Note : Need to Clear by Software.

◆ **UBAUD**(0X151) : ***UART Baud Rate Setting Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UBAUD	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

UBAUD : ***UART Baud Rate value depend on UBAUD Register & UCON Register BAUDS bit.***

Equation : Baud Rate = (Fosc/4) / (UBAUD+1), BAUDS=0;
Baud Rate = (Fosc/16) / (UBAUD+1), BAUDS=1;

Example :
If Fosc = 24M Hz , want to generate 1152000 Hz Baud Rate.
UBAUD= ((24000000/16) / 115200)-1 =12 --> 0x0c
URAUD Register = 0x0C, BAUDS bit =1.

◆ **UBUF**(0X152) : ***UART Data for Transmit or Receive***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UBUF	UBUF7	UBUF6	UBUF5	UBUF4	UBUF3	UBUF2	UBUF1	UBUF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

UBUF7~UBUF0 : ***UART Transmission or Reception Data.***

◆ **SPIRB2**(0X15A) : ***SPI-2 Data Read Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIRB2	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

◆ **SPIWB2**(0X15B) : ***SPI-2 Data Write Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIWB2	WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

SPIRB2 Register is a 8 bits Data Buffer for SPI-2 Data Read In.

SPIWB2 Register is a 8 bits Data Buffer for SPI-2 Data Write Out.

◆ **SPIS2**(0X15C) : ***SPI-2 Status Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIS2	-	-	-	-	ODO	ODC	RBFIF	RBF
R/W-	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

ODO : *SDO Open-Drain Control*

ODO=0 ,SDO Open-Drain Disable.

ODO=1 ,SDO Open-Drain Enable.

ODC : *SCK Open-Drain Control*

ODC=0 ,SCK Open-Drain Disable.

ODC=1 ,SCK Open-Drain Enable.

RBFIF : *SPI Read Buffer Full Interrupt Flag*

RBFIF=1 ,(a)Receive Completed, and Read Buffer is Full.

(b) Under the Interrupt Enable, and Interrupt Occur.

RBFIF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

RBFIF : *SPI Read Buffer Full Flag*

RBF=1 ,Receive Completed, and Read Buffer is Full.

RBF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

◆ **SPIC2**(0X15D) : ***SPI-2 Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIC2	CES	SPIE	SRO	SSE	ORD	SBRS2	SBRS1	SBRS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	-	0	0	0	0

CES : *SPI Clock Edge Selection*

CES=0 , **Low go High** , Data Out; **High go Low** Data In.

CES=1 , **High go Low** , Data Out; **Low go High** Data In.

SPIE : *SPI Enable*

SPIE=0 ,SPI Disable.

SPIE=1 ,SPI Enable.

SRO : *Data In Overflow Flag (Only Used SLAVE Mode)*

SRO=1 ,Last Byte Data in SPI Read Buffer had not Read Out .

SRO=0 ,Otherwise.

SSE : *Start Shift SPI Data Out*

SSE=1 ,(a)Start Shift SPI Data Out.

(b) Completed Working , Clear SSE bit by Hardware .

SRO=0 ,Otherwise.

ORD : *SPI Data Shift Order*

ORD=0 ,MSB Bit First.

ORD=1 ,LSB Bit First.

SBRS2~SBRS0 : *SPI Baud Rate & Mode Selection*

SBRS~SBRS0 : ***Selection bits for Baud Rate & Mode***

SBRS	SBRS1	SBRS0	Mode	Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Slave	SS Enable
1	1	0	Slave	SS Disable
1	1	1	Master	TMR1/2

◆ **INTF** (0x17F) : ***Interrupt Flag Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTF	-	-	-	-	TR1IF	SPIIF	EXIF	TR0IF
R/W					R/W	R/W	R/W	R/W
RESET					0	0	0	0

TR1IF : Timer 1 overflow flag.

TR1IF = 0 , Clear it by Software.

TR1IF = 1 , When Timer 1 overflow , this flag will be set to '1'.

SPIIF : SPI interrupt flag.

SPIIF = 0 , Clear it by Software.

SPIIF = 1 , Will be set when SPI interface interrupt occurred.

EXTIF : External interrupt flag.

EXTIF = 0 , Clear it by Software.

EXTIF = 1 , Will be set when the external interrupt occurred.

TR0IF : Timer 0 overflow flag.

TR0IF = 0 , Clear it by Software.

TR0IF = 1 , When Timer 0 overflow , this flag will be set to '1'.

3.0 Instruction Sets.

3.1 Overview

INSTRUCTION	DESCRIPTION	STATUS AFFECTED
NOP	No Operation	None
MCRW	A ---> CONT	None
MCRR	CONT ---> A	None
DAW	Decimal Adjust A	C
SLEEP	Go into Standby mode	T,P
WDTC	Clear Watchdog Timer	T,P
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
CLRW	Clear A	Z
CLR R	Clear R	Z
INT	PC+1 ---> Top Stack, Jump to 0002H	None
RETURN	Return from Subroutine	None
RETINT	Return from Interrupt	None
RETLW k	Return with literal in A	None
CALL k	Call Subroutine	None
JMP k	Jump to Address	None
MOV R,W	Move A to R	None
MOV W,R	Move R to A	Z
MOV R,R	Move R to R	Z
MOV W,k	Move literal to A	None
MOVC W,k	Move PAL, PAH ROM Data --> A	None
SWAPW R	Swap nibbles in R, ----> A	None
SWAP R	Swap nibbles in R, ----> R	None
BCR R,b	Bit Clear R	None
BSR R,b	Bit Set R	None
BTSC R,b	Bit Test R, Skip if Clear	None
BTSS R,b	Bit Test R, Skip if Set	None
RRCW R	Rotate Right R Through Carry ,----> A	C
RRC R	Rotate Right R Through Carry ,----> R	C
RLCW R	Rotate Left R Through Carry ,----> A	C

3.1 Overview (Continue)

INSTRUCTION	DESCRIPTION	STATUS AFFECTED
RLC R	Rotate Left R Through Carry ,----> R	C
AND W,R	A AND R ---> A	Z
AND R,W	A AND R ---> R	Z
AND W,k	A AND k ---> A	Z
OR W,R	A OR R ---> A	Z
OR R,W	A OR R ---> R	Z
OR W,k	A OR k ---> A	Z
XOR W,R	A XOR R ---> A	Z
XOR R,W	A XOR R ---> R	Z
XOR W,k	A XOR k ---> A	Z
INVW R	/R ---> A	Z
INV R	/R ---> R	Z
ADD W,R	A + R ---> A	Z,C,DC
ADD R,W	A + R ---> R	Z,C,DC
ADD W k	k+A ---> A	Z,C,DC
SUB W,R	R-A ---> A	Z,C,DC
SUB R,W	R-A ---> R	Z,C,DC
SUB W,k	k-A ---> A	Z,C,DC
INCW R	R+1 ---> A	Z
INC R	R+1 ---> R	Z
DECW R	R-1 ---> A	Z
DEC R	R-1 ---> R	Z
IRSZW R	R+1 ----> A, Skip if A=0	None
IRSZR R	R+1 ----> A, Skip if R=0	None
DRSZW R	R-1 ---> A, Skip if A=0	None
DRSZR R	R-1 ---> R, Skip if R=0	None

3.2 General Control Instructions

NOP	*No Operation*
Operation	NOP
Instruction Cycle	2
Affected Flag	None
Description	No any operation
Example	NOP

MCRW	*Writer W Register to MCR Register*
Operation	W --> MCR
Instruction Cycle	2
Affected Flag	None
Description	Copy W Register Data to MCR Register
Example	; before W = 10, MCR=15 MCRW ; after W=10, MCR=10

MCRR	*Writer MCR Register to W Register*
Operation	MCR --> W
Instruction Cycle	2
Affected Flag	None
Description	Copy MCR Register Data to W Register
Example	; before W = 10, MCR=15 MCRR ; after W=15, MCR=15

DAW	*Decimal Adjust*
Operation	If W[3:0]>9 or DC=1 Then W[3:0]+6 --> W[3:0] If W[7:4]>9 or C=1 Then W[7:4]+6 --> W[7:4]
Instruction Cycle	2
Affected Flag	C
Description	W Register Decimal Adjust & Place Result in W Register
Example	MOV W,@0x0E ; W=0x0EH DAW ; W=0x14H

SLEEP	*Sleep*
Operation	0--> WDT; Oscillator Stop
Instruction Cycle	2
Affected Flag	T,Z
Description	Clear Watch Dog Timer; then MCU Sleep
Example	SLEEP

WDTC	*Watch Dog Timer Clear*
Operation	0--> WDT;
Instruction Cycle	2
Affected Flag	T,P
Description	Clear Watch Dog Timer
Example	WDTC

ENI	*Enable Interrupt*
Operation	MCR/GIE Flag=0
Instruction Cycle	2
Affected Flag	None
Description	Enable Interrupt
Example	DISI

DISI	*Disable Interrupt*
Operation	MCR/GIE Flag=1
Instruction Cycle	2
Affected Flag	None
Description	Disable Interrupt
Example	DISI

CLR W	*Clear Working Register*
Operation	0 --> W
Instruction Cycle	2
Affected Flag	Z=1
Description	Clear Working Register Content --> W=0
Example	; before W=5AH CLR W ; after W=0H

CLR R	*Clear Register*
Operation	0 --> R
Instruction Cycle	2
Affected Flag	Z=1
Description	Clear Register Content --> R=0
Example	; before 0x10=5AH CLR 0x10 ; after 0x10=0H

INT	*Software Interrupt*
Operation	0001H --> PC, (PC+1) --> (Top Stack)
Instruction Cycle	4
Affected Flag	None
Description	Software Interrupt, go to 0001H Address(PC); Push the PC+1 to Top Stack
Example	ORG 0001H JMP SF_INT NOP SF_INT: NOP RETINT ; Feedback to LAB1 Main: NOP **INT** ; Software Interrupt ; go to 0001H Addr. LAB1 NOP ; ; Push LAB1 to Top Stack

3.3 Flow Control Instructions

RETURN	***Return from Subroutine.***
Operation	(Top Stack)--> PC,
Instruction Cycle	4
Affected Flag	None
Description	Return from Subroutine ; POP The Address from Top Stack
Example	SUB2: ; Subroutine 2. NOP NOP **RET** ; Return to LAB4 Addr. ; LAB3: NOP NOP CALL SUB2 ; go to SUB2 LAB4: NOP

RETINT	***Return from Interrupt.***
Operation	(Top Stack)--> PC, MCR/GIE Flag=1
Instruction Cycle	4
Affected Flag	None
Description	Return from Interrupt ; POP The Address from Top Stack
Example	ORG 0001H JMP SF_INT NOP SF_INT: NOP **RETINT** ; Feedback to LAB1 Main: NOP INT ; Software Interrupt ; go to 0001H Addr. LAB1 NOP ; ; Push LAB1 to Top Stack

RETLW	*Return with literal in W(Accumulator).*
Operation	(Top Stack)--> PC, MCR/GIE Flag=1
Instruction Cycle	4
Affected Flag	None
Description	Return from Interrupt ; POP The Address from Top Stack
Example	ORG 0001H JMP SF_INT NOP SF_INT: NOP **RETINT** ; Feedback to LAB1 Main: NOP INT ; Software Interrupt ; go to 0001H Addr. LAB1 NOP ; ; Push LAB1 to Top Stack

CALL k	*Call Subroutine*
Operation	K --> PC, (PC+1) --> (Top Stack)
Instruction Cycle	4
Affected Flag	None
Description	Call Subroutine, go to k Address(PC); Push the PC+1 to Top Stack
Example	**CALL** SUB1 ; go to SUB1 Addr. NOP NOP SUB1: ;

JMP k	*Jump to Assigned Addr.*
Operation	K --> PC,
Instruction Cycle	4
Affected Flag	None
Description	Go to k Address(PC);
Example	**JMP** LAB2 ; go to LAB2 Addr. NOP NOP LAB2: ;

3.4 Data Move Instructions

MOV R, W	*Write W Register to R Register*
Operation	W --> R
Instruction Cycle	2
Affected Flag	None
Description	Copy W Register Data to R Register
Example	NOP ; before W = 10, 0x20=0 MOV 0x20, W ; after W=10 , 0x20=10

MOV W, R	*Write R Register to W Register*
Operation	R --> W
Instruction Cycle	2
Affected Flag	Z
Description	Copy R Register Data to W Register
Example	NOP ; before W = 10, 0x25=15 MOV W, 0x25 ; after W=15 , 0x25=15

MOV R, R	*Writer R Register to itself*
Operation	R --> R
Instruction Cycle	2
Affected Flag	Z
Description	Copy R Register Data to R Register For check R Register is Zero or Not If Zero then Z flag=1

Example	; before 0x20=10
	..... ; 0x21=0
	MOV 0x20, 0x20 ; 0x20=10, Z=0
	MOV 0x21, 0x21 ; 0x21=0, Z=1

MOV W, k	*Writer a constant to W Register*
Operation	k --> W
Instruction Cycle	2
Affected Flag	None
Description	Copy W Register Data to R Register

Example	; before W = 10
	MOV W, @0x12 ; after W=12H
	MOV W, @01001010 ; W=4AH

MOVC	*Write ROM Data to W Register*
Operation	ROM Addr. [6:0]=PAL[7:1] ROM Addr. [11:7]=PAH[5:0] if PAL[0]='0'b then ROM[7:0]-->W if PAL[0]='1'b then ROM[15:8]-->W
Instruction Cycle	2
Affected Flag	None
Description	Read the ROM Data to W Register

Example	NOP ; Read Addr 100H ROM Data
	; ROM Addr.100H=0x1234
	
	MOV W,@0x00 ;
	MOV PAL,W
	MOV W,@0x02
	MOV PAH,W
	MOVC ;W=0x34 Read Low Byte
	MOV W@0x01
	MOV PAL,W
	MOVC ;W=0x12 Read High Byte

SWAPW R	*Swap R; Place Result in W Register*
Operation	R[3:0] --> W[7:4], R[7:4] --> W[3:0]
Instruction Cycle	2
Affected Flag	None
Description	Swap R Register High Nibble and Low Nibble & Place Result in W Register
Example	; before W = 10, 0x10=5A SWAPW 0x10 ; after W=A5, 0x10=5A

SWAP R	*Swap R*
Operation	R[3:0] <--> R[7:4]
Instruction Cycle	2
Affected Flag	None
Description	Swap R Register High Nibble and Low Nibble & Place Result in R Register
Example	; before 0x10=5A SWAPW 0x10 ; after 0x10=A5

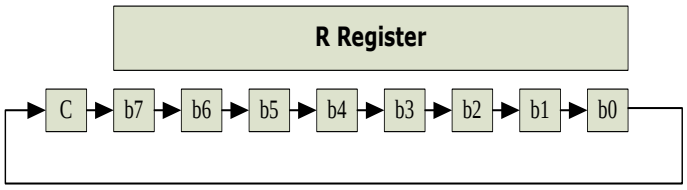
3.5 Bit Operate Instructions

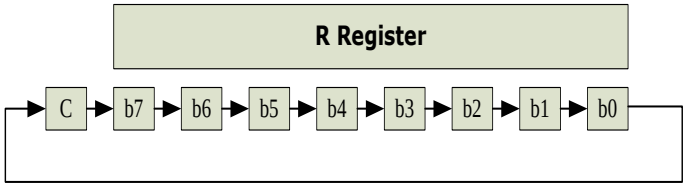
BCR R, b	*Clear Bit of Register*
Operation	0 --> R[b]
Instruction Cycle	2
Affected Flag	None
Description	Clear Assigned Bit of Register R[b]='0'b
Example	; before 0x10=5AH BCR 0x10,3 ; after 0x10=52H

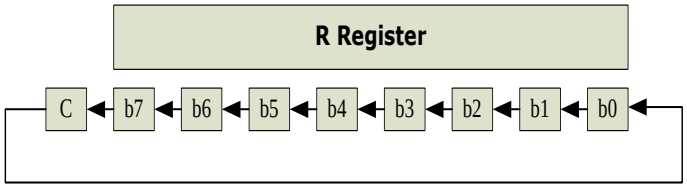
BSR R, b	*Set Bit of Register*
Operation	1 --> R[b]
Instruction Cycle	2
Affected Flag	None
Description	Set Assigned Bit of Register R[b]='1'b
Example	; before 0x10=5AH BSR 0x10,2 ; after 0x10=5EH

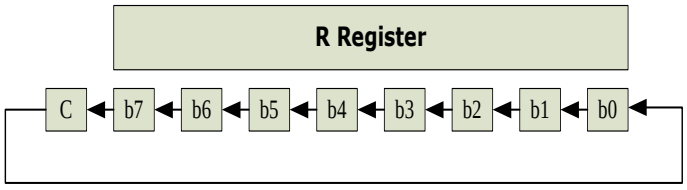
BTSC R, b	*Bit Test, Skip if Clear*
Operation	if R[b]=0 then Skip
Instruction Cycle	4
Affected Flag	None
Description	Bit Test; If this Bit is Clear, then Skip next instruction.
Example	; 0x20=01011010b ; 0x20 Bit2 ='0'b **BTSC** 0x20,2 ;Skip to NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

BTSS R, b	*Bit Test, Skip if Set*
Operation	if R[b]=1 then Skip
Instruction Cycle	4
Affected Flag	None
Description	Bit Test; If this Bit is Set, then Skip next instruction.
Example	; 0x20=01011010b ; 0x20 Bit3 ='1'b **BTSS** 0x20,1 ;Skip to NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

RRCW R	*Rotate Right R through Carry*
Operation	R[n]->W[n-1], R[0]->C, C--> W[7]
Instruction Cycle	2
Affected Flag	C
Description	 Place The Result in W Register
Example	; before W=0H , 0x10=5AH,C=1 RLCW 0x10 ; after W=ADH , 0x10=5AH,C=0

RRC R	*Rotate Right R through Carry*
Operation	R[n]->R[n-1], R[0]->C, C--> R[7]
Instruction Cycle	2
Affected Flag	C
Description	 Place The Result in R Register
Example	; before W=0H , 0x10=5AH,C=1 RLCW 0x10 ; after W=0H , 0x10=ADH,C=0

RLCW R	*Rotate Left R through Carry*
Operation	R[n]->W[n+1], R[7]->C, C--> W[0]
Instruction Cycle	2
Affected Flag	C
Description	 Place The Result in W Register
Example	; before W=0H , 0x10=5AH,C=1 RLCW 0x10 ; after W=B5H , 0x10=5AH,C=0

RLC R	*Rotate Left R through Carry*
Operation	R[n]->R[n+1], R[7]->C, C--> R[0]
Instruction Cycle	2
Affected Flag	C
Description	 Place The Result in R Register
Example	; before W=0H , 0x10=5AH,C=1 RLC 0x10 ; after W=0H , 0x10=B5H,C=0

3.6 Boolean Operate Instructions

AND W, R	*And logical operation*
Operation	W & R --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register & R Register & Place Result in W Register
Example	; before 0x10=5AH, W=0FH AND W,0x10 ; after 0x10=5AH, W=0AH

AND R, W	*And logical operation*
Operation	W and R --> R
Instruction Cycle	2
Affected Flag	Z
Description	W Register and R Register & Place Result in R Register
Example	; before 0x10=5AH, W=0FH AND 0x10, W ; after 0x10=0AH, W=0FH

AND W, k	*And logical operation*
Operation	W and k --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register and Constant k & Place Result in W Register
Example	; before W=A5H AND W, @0x0F ; after W=05H

OR W, R	*Inclusive OR logical operation*
Operation	W or R --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register or R Register & Place Result in W Register
Example	; before 0x10=5AH, W=0FH OR W,0x10 ; after 0x10=5AH, W=5FH

OR R, W	*Inclusive OR logical operation*
Operation	W or R --> R
Instruction Cycle	2
Affected Flag	Z
Description	W Register or R Register & Place Result in R Register
Example	; before 0x10=5AH, W=0FH OR 0x10, W ; after 0x10=5FH, W=0FH

OR W, k	*Inclusive OR logical operation*
Operation	W or k --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register or Constant k & Place Result in W Register
Example	; before W=A5H AND W, @0x0F ; after W=AFH

XOR W, R	*Exclusive OR logical operation*
Operation	W xor R --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register or R Register & Place Result in W Register
Example	; before 0x10=5AH, W=0FH XOR W,0x10 ; after 0x10=5AH, W=55H

XOR R, W	*Exclusive OR logical operation*
Operation	W xor R --> R
Instruction Cycle	2
Affected Flag	Z
Description	W Register xor R Register & Place Result in R Register
Example	; before 0x10=5AH, W=0FH XOR W,0x10 ; after 0x10=55H, W=0FH

XOR W, k	*Exclusive OR logical operation*
Operation	W xor k --> W
Instruction Cycle	2
Affected Flag	Z
Description	W Register xor Constant k & Place Result in W Register
Example	; before W=A5H AND W, @0x0F ; after W=AAH

3.7 Arithmetic Operate Instructions

INVW R	*Inverse Working Register*
Operation	/R --> W
Instruction Cycle	2
Affected Flag	Z
Description	Inverse Working Register Content W=/R
Example	; before W=0H ,0x10=5AH INVW 0x10 ; after W=A5H,0x10=5AH

INV R	*Inverse R Register*
Operation	/R --> R
Instruction Cycle	2
Affected Flag	Z
Description	Inverse Working Register Content W=/R
Example	; before W=0H , 0x10=5AH INV 0x10 ; after W=0H , 0x10=A5H

ADD W, R	*Add*
Operation	W+R --> W
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 C=1 ; when the bit7 is Overflow DC=1; When the bit3 is Overflow
Description	W Register add R Register & Place Result in W Register

Example	; For R10 + R11--> W
	MOV W, 0x10 ; W=R10
	ADD W, 0x11 ; W=R10 +R11

ADD R, W	*Add*
Operation	W+R --> R
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 C=1 ; when the bit7 is Overflow DC=1; When the bit3 is Overflow
Description	W Register add R Register & Place Result in R Register

Example	; For R10 + R11--> R11
	MOV W, 0x10 ; W=R10
	ADD 0x11, W ; R11=R10 +R11

ADD W, k	*Add*
Operation	W+k --> W
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 C=1 ; when the bit7 is Overflow DC=1; When the bit3 is Overflow
Description	W Register add a constant & Place Result in W Register

Example	; For R10 + 15H --> W
	MOV W, 0x10 ; W=R10
	ADD W, @0x15 ; W=R10 +15H

SUB W, R	*Subtract*
Operation	R-W --> W
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 ***C=0 ; when the bit7 is Overflow*** ***DC=0; When the bit3 is Overflow***
Description	R Register subtract W Register & Place Result in W Register

Example	; For R11- R10 --> W
	MOV W, 0x10 ; W=R10
	SUB W, 0x11 ; W=R11 – R10

SUB R, W	*Subtract*
Operation	R-W --> R
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 ***C=0 ; when the bit7 is Overflow*** ***DC=0; When the bit3 is Overflow***
Description	R Register subtract W Register & Place Result in R Register

Example	; For R11- R10--> R11
	MOV W, 0x10 ; W=R10
	SUB 0x11, W ; R11=R11 -R10

SUB W, k	*Subtract*
Operation	k-W --> W
Instruction Cycle	2
Affected Flag	Z,C,DC Z=1 ; when the Result =0 ***C=0 ; when the bit7 is Overflow*** ***DC=0; When the bit3 is Overflow***
Description	A Constant subtract W Register & Place Result in W Register

Example	; For 15H – R10 --> W
	MOV W, 0x10 ; W=R10
	ADD W, @0x15 ; W=15H – R10

INCW R	*Increment R*
Operation	R+1 --> W
Instruction Cycle	2
Affected Flag	Z
Description	R Register Content add 1 & Place Result in W Register
Example	; before 0x10=5AH, W=0 INCW 0x10 ; after 0x10=5AH, W=5BH

INC R	*Increment R*
Operation	R+1 --> R
Instruction Cycle	2
Affected Flag	Z
Description	R Register Content add 1 & Place Result in R Register
Example	; before 0x10=5AH INC 0x10 ; after 0x10=5BH

DECW R	*Decrement R*
Operation	R-1 --> W
Instruction Cycle	2
Affected Flag	Z
Description	R Register Content subtract1 & Place Result in W Register
Example	; before 0x10=5AH, W=0 DECW 0x10 ; after 0x10=5AH, W=59H

DEC R	*Decrement R*
Operation	R-1 --> R
Instruction Cycle	2
Affected Flag	Z
Description	R Register Content subtract 1 & Place Result in R Register
Example	; before 0x10=5AH DEC 0x10 ; after 0x10=59H

IRSZW R	*Increment R, Skip if Zero.*
Operation	(R+1)-->W , Skip if result = 0
Instruction Cycle	4
Affected Flag	None
Description	Decrement R & Place the Result in W; If (R+1)=0 then Skip next instruction.
Example	; before 0x20=FFH **IRSZW** 0x20 ;W=0H,Skip NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

IRSZR R	*Increment R, Skip if Zero.*
Operation	(R+1)-->R , Skip if result = 0
Instruction Cycle	4
Affected Flag	None
Description	Increment R & Place the Result in R; If (R+1)=0 then Skip next instruction.
Example	; before 0x20=FFH **IRSZR** 0x20 ;0x20=0H,Skip NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

DRSZW R	*Decrement R, Skip if Zero.*
Operation	(R-1)-->W , Skip if result = 0
Instruction Cycle	4
Affected Flag	None
Description	Decrement R & Place the Result in W; If (R-1)=0 then Skip next instruction.
Example	; before 0x20=01H **DRSZW** 0x20 ;W=0H,Skip NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

DRSZR R	***Decrement R, Skip if Zero.***
Operation	(R-1)-->R , Skip if result = 0
Instruction Cycle	4
Affected Flag	None
Description	Decrement R & Place the Result in R; If (R-1)=0 then Skip next instruction.
Example	; before 0x20=01H **DRSZR** 0x20 ;0x20=0H,Skip NEXT2 NEXT1: JMP LAB1 NEXT2: JMP LAB2 LAB1: MOV W,@0AH LAB2: MOV W,@0BH ;

4.0 Device Configuration Options.

4.1 Protection

YSM146 have protection option to protect the code in MCU OTP ROM. If the protection option had been armed, there is no way to read back the data from OTP ROM.

4.2 Warm-up time

While the MCU is booting up, it will delay for specific time to wait for system stable. User can set up the time according to the slowest device in whole system to prevent timing issue error.

4.3 Power Save Mode(Eco-Mode)

YSM146 can reduce the power consumption by setting up this option. But limitation are existed for specific Eco-Mode level.

The system frequency should lower than 12MHz for Eco-Mode level-1, and lower than 500KHz for Eco-Mode level-2.

4.4 LDO (Low Drop Regulator)

YSM146 had an LDO module which can made the chip core operate in more wide range of the voltage. But the power consumption will little higher if the LDO module was being enabled.

4.5 System clock source selection

YSM146 had 6 types of the system clock source:

1. XTH – High speed external crystal (Frequency > 1MHz)
2. XTL – Low Speed external crystal (Frequency < 1MHz)
3. IRC w/o OSCO – Internal RC mode, no any outgoing clocks signal.
4. IRC w OSCO – Internal RC mode with the clock out on OSCO.
5. Ext.RC w/o OSCO – External RC mode, no any outgoing clocks.
6. Ext.RC w OSCO – External RC mode with the clock out on OSCO.

Notes. OSCO frequency will be half from system frequency.

Ex. If Fosc=12MHz, the frequency from OSCO will be 6MHz.

4.6 Low Voltage Reset

YSM146 had an Low Voltage Reset module, which can self reset the MCU if the operating voltage is lower than specific voltage level. User can specific the reference voltage and the continuous time period. If the voltage was below the reference voltage and keep for an period of the user specific, MCU will reset to avoid the low voltage issue error.

4.7 General MCU Functions

There are the following general MCU function can be setting in device configuration option.

1. Watch Dog Timer : There is an internal RC clocked timer for watch dog function.

2. I/O Drive Enhance : I/O ports can enhance the driving ability by setting up this option, but the power consumption will rise higher.

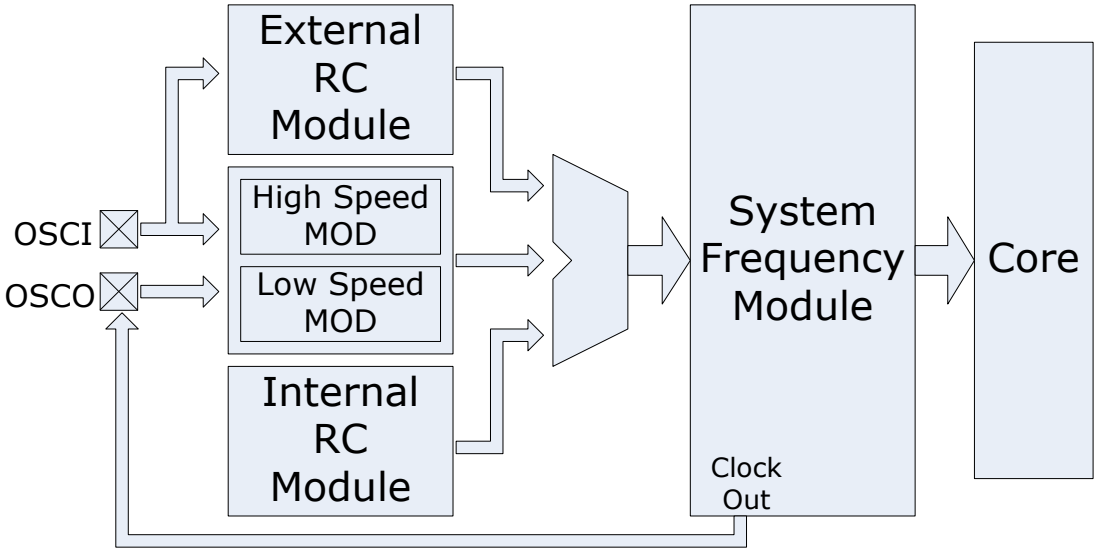
3. Auto Pull Setting : YSM146 have internal Pull up/down resistor for I/O ports. But if the output ports with internal pull up/down resistor connected, it will have the current leaking. If the Auto Pull Setting had been set, MCU will disconnect the pull up/down resistor while the ports being set to output to avoid the current leaking.

4. PF3 / External Interrupt : User can select the PF3 as normal I/O pin or external interrupt pin.

5. PF5 / RSTN : PF5 pin can be set as normal pin or reset pin.

5.0 System Clock.

5.1 System clock overview



5.2 Clock source type

YSM146 have 3 different types of the clock source:

1. External crystal
2. Internal RC
3. External RC

5.3 External Crystal

User can use the standard 2 pins crystal(XTAL) with the internal clocking circuit to generate the precise frequency. The frequency can reach up to 16MHz.

5.4 Internal RC

YSM146 had build in an RC frequency generator on chip. User can select this module to generate an frequency clock signal for core use. It's no need to add any additional device to generate the clock signal. User can setting up to export the generated clock signal out from OSCO pin or not by device configuration.

5.5 External RC

Except to the chip build-in RC frequency clock generator, user can connect to an RC circuit outside the chip from OSCI pin instead of the internal RC circuit. In this mode, user can adjust the external RC circuit to change the clock frequency. It's also can export the generated clock signal out from the OSCO pin.

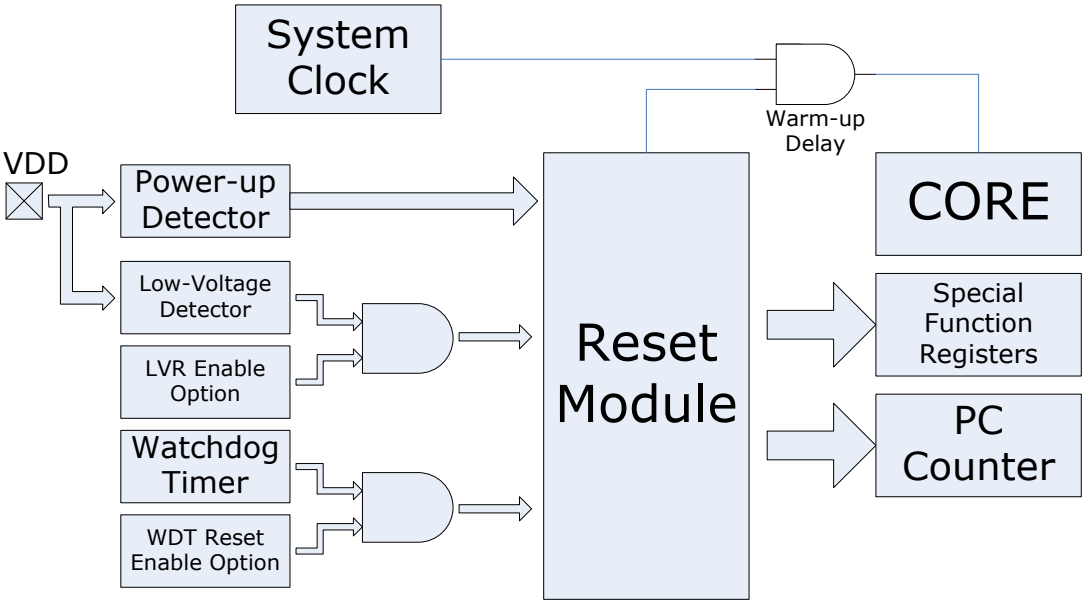
5.6 Clock signal export

YSM146 have an clock export module which can export an half frequency clock signal from the OSCO pin. This function was defined on the device configuration option.

Ex. If the system clock frequency = 12MHz, Clock signal export from OSCO will be 6MHz clock signal.

6.0 Reset Module.

6.1 Overview



6.2 Power-On Reset

While the MCU had been power up, the MCU reset module will delay with the specific time period and reset the special function registers at the same time. The PC counter will also reset to address 0xFFF while the power on reset. User can adjust the power up delay period (warm-up time) to wait the slower device in the designed system to avoid the timing issue error.

6.3 Low Voltage Reset (L.V.R)

M146 had build-in an low voltage detector. If the operating voltage (VDD)'s level is keep below the specific reference voltage level for an specific period, low voltage detector will send an reset signal to the reset module to reset the MCU. This function is used to avoid the operating error from the low voltage issue. If the LVR reset had been executed, the PC counter will be reset to 0xFFF.

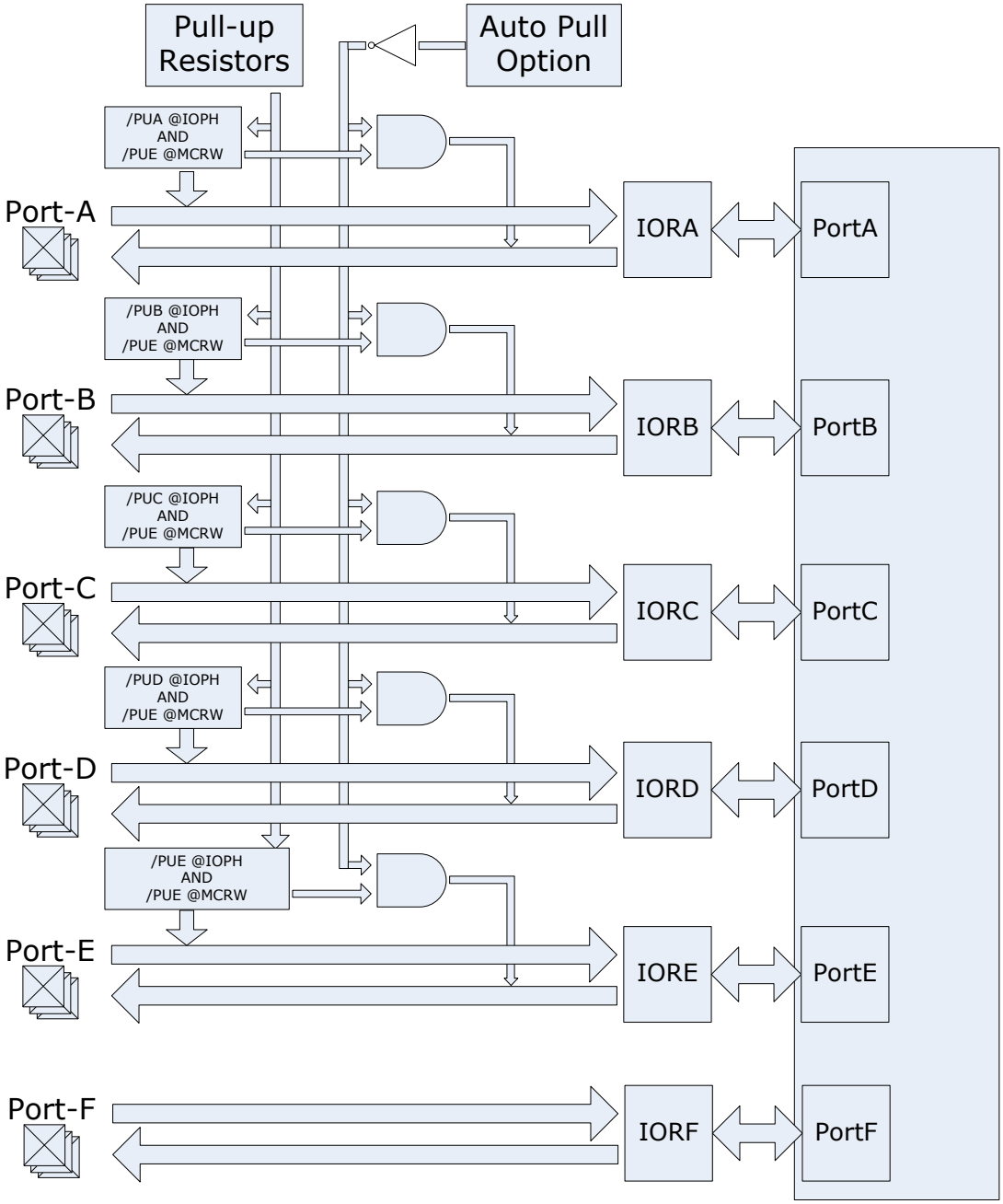
6.4 Watchdog Reset (WDT Reset)

YSM146 had a watchdog timer. If the watchdog timer had been enable and the watchdog timer overflow flag was being set, it will send an reset signal to reset module to reset the MCU. The PC counter will be reset to 0xFFF. The watchdog timer reset is used to avoid the MCU hang on crash or infinite looping status.

Notes: User should clear up the watch dog timer regularly to avoid the WDT reset.

7.0 I/O Ports Module.

7.1 Overview



7.2 Ports

M146 have 6 I/O ports, which are Port-A, Port-B, Port-C, Port-D, Port-E and Port-F. Each port can be set to input or output. Except Port-C is 6bits wide, all the other ports are 8bits wide. All ports can connect with the internal pull resistors.

There are 3 general power relative ports(VDD / VDDL / VSS)

1 External reset port are available, low active.

1 External interrupt pin with internal pull up.

2 frequency ports (OSCI / OSCO)

16 A/D input channels (A/D converter)

1 analog output channel(current D/A converter)

7.3 I/O Ports Direction Control

There are 6 ports in YSM146. Each one can be set to input or output by using the IORx special function register to control the port direction.

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IORA	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1
IORB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1
IORC	-	-	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
RESET	-	-	1	1	1	1	1	1
IORD	IOD7	IOD6	IOD5	IOD4	IOD3	IOD2	IOD1	IOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1
IORE	IOE7	IOE6	IOE5	IED4	IOE3	IOE2	IOE1	IOE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	1	1	1	1	1

(Continue)

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IORF	IOF7	IOF6	IOF5	IOF4	IOF3	IOF2	IOF1	IOF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

IOx0~7=0 , as a Output. / IOx0~7=1 , as a Input.

7.4 I/O Ports Value Read/Write

User can read or output the port data via the PORTx special function registers.

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0
PORTB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0
PORTC			PC5	PC4	PC3	PC2	PC1	PC0
R/W			R/W	R/W	R/W	R/W	R/W	R/W
RESET			0	0	0	0	0	0
PORTD	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0
PORTE	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0
PORTF	PF7	PF6	PF5	PF4	PE3	PE2	PE1	PE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

7.5 I/O Ports Pull resistors

◆ **MCRW** (0x122) : ***Main Control Register for Write***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCRR	/PUE	GIE	-	-	PAB	PS2	PS1	PS0
R/W	R/W	R/W			R/W	R/W	R/W	R/W
RESET								

/PUE : ***I/O Port Pull-Up Resistor Enable*** .

/PUE=0 : I/O Connected with Pull-Up Resistor.

/PUE=1 : Pull-Resistor Disconnected.

◆ **IOPH** (0x12D) : ***I/O Port Pull High Register***

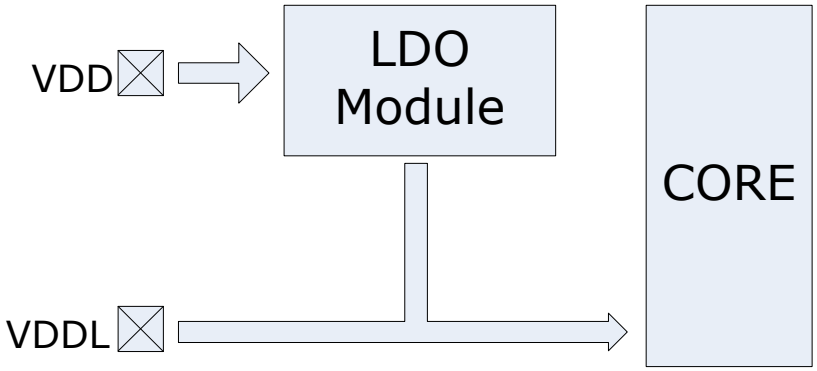
NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IOPH	SSPC	-	-	/PUC	/PUE	/PUD	/PUB	/PUA
R/W	R/W	-	-	R/W	R/W	R/W	R/W	R/W
RESET								

/PUA~E : *Each I/O Port Pull-High Enable Bit*

/PUA~E=0 , Enable (Connected with pull high Resistor).

/PUA~E=1 , Disable.

7.6 Power Relative Pins



VDD and VDDL should connect to an 0.1uF capacitor each.

7.7 External Interrupt Pin

User can trig the external interrupt by set low to the external interrupt pin with internal pull up.

8.0 Chip Status.

8.1 Overview

The status flags are being build in the YSM146's special function registers. User can know the status of the MCU by monitor the register.

8.2 Status Register

◆ **STATUS** (0x103) : ***Status Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STATUS	GPR	-	-	/TO	/PD	Z	DC	C
R/W	R/W			R/W	R/W	R/W	R/W	R/W
RESET								

GPR : ***General Purpose Read/Write bit***

/TO : ***Time- Out Flag***

/TO=0 Watch dog Timer Overflow.

/TO=1 (a) Power On

(b) Execute WDTC or SLEEP Instruction.

/PD : ***Power Down Flag***

/PD=0 After SLEEP Instruction.

/PD=1 (a) Power On

(b) Execute WDTC Instruction.

Z : ***ALU Operation Zero Flag***

Z=0 Operation Result is not Zero.

Z=1 Operation Result is Zero.

DC : ***ALU Operation Half Carry /Borrow Flag***

DC=0 Half Carry/Borrow does not occur.

DC=1 Half Carry/Borrow occurred.

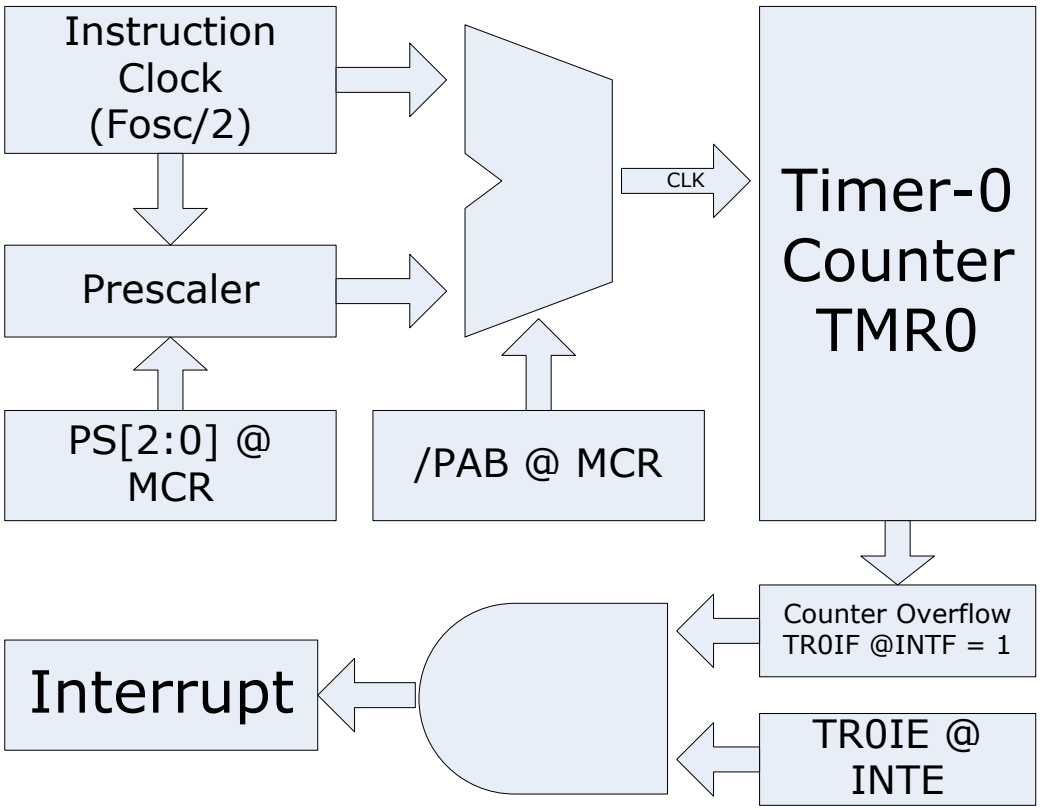
C : ***ALU Operation Carry /Borrow Flag***

C=0 Carry/Borrow does not occur.

C=1 Carry/Borrow occurred.

9.0 Timer0.

9.1 Overview



9.2 Registers

◆ **MCRW** (0x122) : ***Main Control Register for Write***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCRR	/PUE	GIE	-	-	PAB	PS2	PS1	PS0
R/W	R/W	R/W			R/W	R/W	R/W	R/W
RESET	1	0			1	1	1	1

PAB : ***Prescaler bit Assignment .***

PAB=0 Assign to TMR0 (Timer 0).

PAB=1 Assign to WDT (Watch-Dog Timer).

PS2~PS0 : ***Prescaler bits.***

PS2	PS1	PS0	TMR0 Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

When The TMR0 from 0xff increasing to 0x00 , TR0IF will be set to '1', and if the TR0IE=1 , then the Program Counter will go to Address 0x001(Hardware Interrupt Address).

◆ **TMR0** (0x101) : ***8Bits Real Timer Clock/Counter***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMR0	8 bit Real Time Clock / Counter							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

TMR0 : Increased By Instruction Cycle.

◆ **INTE** (0x12F) : ***Hardware Interrupt Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTE	-	-	-	-	TR1IE	SPIIE	EXIE	TR0IE
R/W	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

TR0IE : *Timer 0 Interrupt Enable*

TR0IE=0 , Timer 0 Interrupt Disable .

TR0IE=1 , Timer 0 Interrupt Enable .

◆ **INTF** (0x17F) : ***Interrupt Flag Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTF	-	-	-	-	TR1IF	SPIIF	EXIF	TR0IF
R/W	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

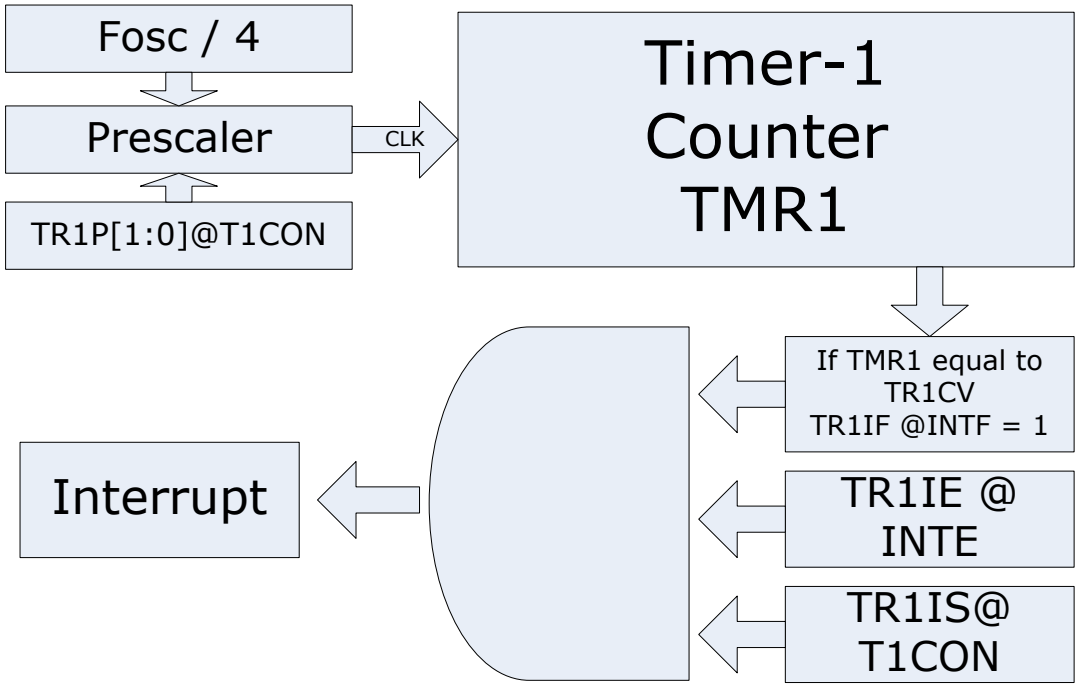
TR0IF : Timer 0 overflow flag.

TR0IF = 0 , Clear it by Software.

TR0IF = 1 , When Timer 0 overflow , this flag will be set to '1'.

10.0 Timer1.

10.1 Overview



10.2 Registers

Timer1 is an 8 bits timer. When set the TR1IE=1, TR1S=1 , the Timer1 will count from 0x00(TMR1).

If the Register TMR1 equal to the register TR1CV, the TR1IF will be set to 1 and the program counter will go to Address 0x001(Hardware Interrupt Address) .

◆ **INTE** (0x12F) : ***Hardware Interrupt Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTE	-	-	-	-	TR1IE	SPIIE	EXIE	TR0IE
R/W	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

TR1IE : *Timer 1 Interrupt Enable*

TR1IE=0 , Timer 1 Interrupt Disable .

TR1IE=1 , Timer 1 Interrupt Enable .

◆ **INTF** (0x17F) : ***Interrupt Flag Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTF	-	-	-	-	TR1IF	SPIIF	EXIF	TR0IF
R/W	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

TR1IF : Timer 1 overflow flag.

TR1IF = 0 , Clear it by Software.

TR1IF = 1 , When Timer 0 overflow , this flag will be set to '1'.

◆ **TMR1** (0x13E) : ***Timer 1 Value Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TMR1	Timer 1 Value Register							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

◆ **TR1CV** (0x13F) : ***Timer 1 Comparator Value Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TR1CV	Timer 1 Comparator Value Register							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET								

◆ **T1CON** (0x12C) : ***Timer 1 Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
T1CON	-	-	-	-	-	TR1S	TR1P1	TR1P0
R/W						R/W	R/W	R/W
RESET								

TR1S : *Timer 1 Turn On Bit*

TR1S=0 , Timer 1 turn off.

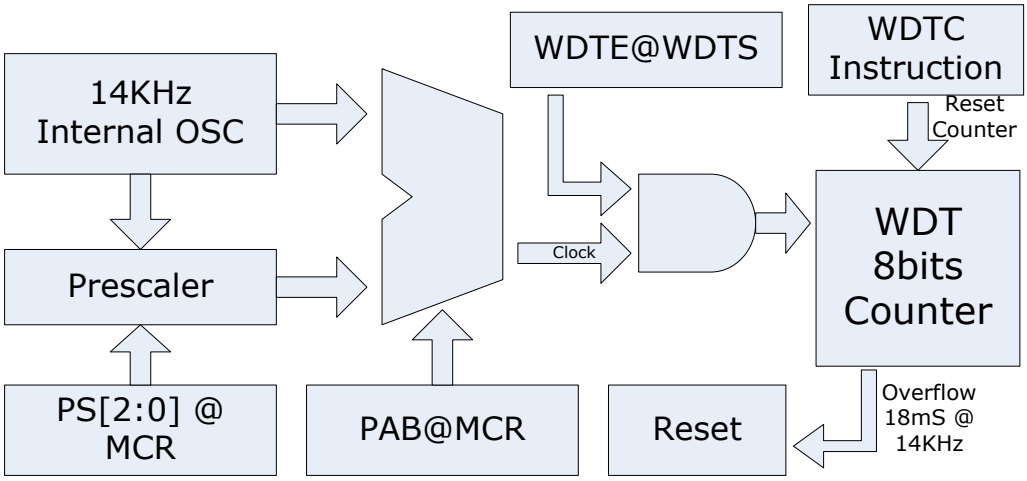
TR1S=1 , Timer 1 turn on.

TR1P1,TR1P0 : *Timer 1 Prescaler Rate*

TR1P1	TR1P0	TMR0 Rate
0	0	1:1
0	1	1:4
1	0	1:8
1	1	1:16

11.0 Watchdog Timer.

11.1 Overview



11.2 Registers

◆ **MCRW** (0x122) : ***Main Control Register for Write***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCRW	/PUE	GIE	-	-	PAB	PS2	PS1	PS0
R/W	R/W	R/W			R/W	R/W	R/W	R/W
RESET	1	0			1	1	1	1

PAB : ***Prescaler bit Assignment .***

PAB=0 Assign to TMR0 (Timer 0).

PAB=1 Assign to WDT (Watch-Dog Timer).

PS2~PS0 : ***Prescaler bits.***

PS2	PS1	PS0	TMR0 Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

◆ **WDTS** (0x12E) : ***Watch Dog & Wake Up Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WDTS	-	ODE	WDTE	SLP2E	-	-	-	/WUE
R/W	-	R/W	R/W	R/W	-	-	-	R/W
RESET								

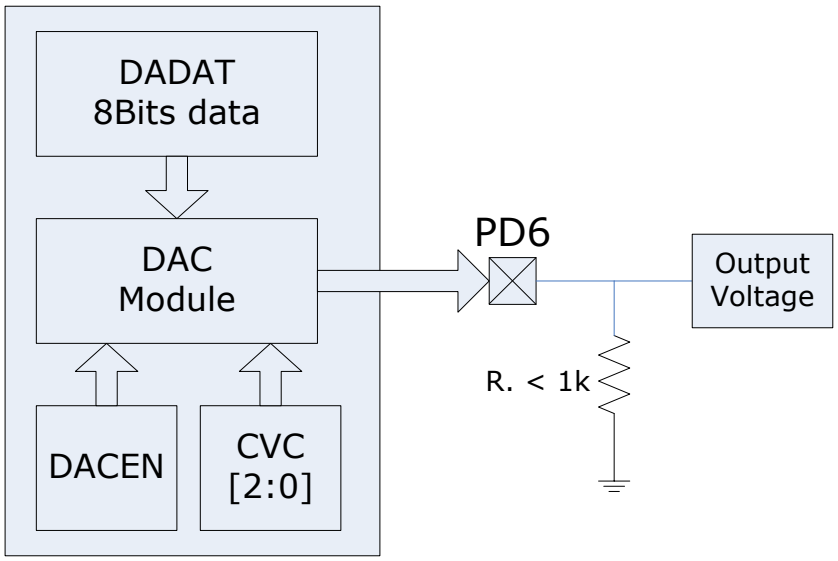
/WDTE : Watchdog timer Enable

/WDTE=0 , Watchdog timer disable .

/WDTE=1 , Watchdog timer enable.

12.0 Current Digital to Analog Converter.

12.1 Overview



12.2 Registers

◆ **DACR** (0x14D) : ***DAC Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DACR	DAEN	-	CVC2	CVC1	CVC0	-	-	-
R/W	R/W	-	R/W	R/W	R/W	-	-	-
RESET	0	-	0	0	0	-	-	-

DAEN : ***DAC Enable Bit***

DAEN=0 , DAC Disable.

DAEN=1 , DAC Enable.

CVC2~CVC0 : Current Level Setting

CVC2~CVC0=0;0;0 , DAC current = Off.

CVC2~CVC0=1;0;0 , DAC current = 1X.

CVC2~CVC0=0;0;0 , DAC current = 2X.

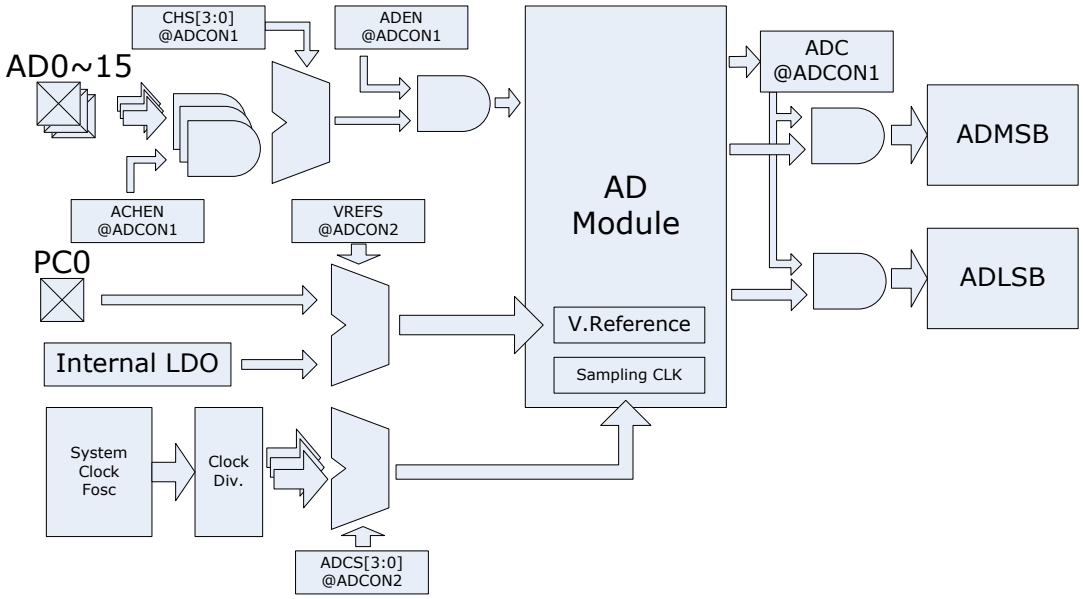
◆ **DADAT** (0x14E) : ***DAC Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DADAT	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

DAC7~DAC0 : ***8 bits Digital Data***

13.0 Analog to Digital Converter.

13.1 Overview



13.2 Registers

◆ **ADCON1**(0X140) : ***A/D Control Register #1***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADCON1	ADC	ADEN	ACHEN	-	CHS3	CHS2	CHS1	CHS0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
RESET	0	0	0	-	0	0	0	0

ADC : *ADC Start Transfer & Completed Flag*

ADC=0 , ADC is be Transfer Completed.(Clear by MCU Hardware)

ADC=1 , ADC Start Transfer.

ADEN : *ADC Converter Enable*

ADEN=0 , ADC Converter Disable.

ADEN=1 , ADC Converter Enable.

ACHEN : *ADC Converter Channel Enable*

ACHEN=0 , ADC Converter Channel Disable.

ACHEN=1 , ADC Converter Channel Enable.

CHS3~CHS0 : *ADC Channel Selection*

CHS3~CHS0 = Channel 15~0.

◆ **ADLSB**(0X141) : ***A/D Digital Data LSB 2bits of 10bits***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADLSB	AD01	AD00	-	-	-	-	-	-
R/W	R/W	R/W	-	-	-	-	-	-
RESET	0	0	-	-	-	-	-	-

AD09~AD02 : ***ADC Transfer to Digital Data bit9~bit0***

◆ **ADMSB**(0X142) : ***A/D Digital Data MSB 8bits of 10bits***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADMSB	AD09	AD08	AD07	AD06	AD05	AD04	AD03	AD02
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

AD09~AD02 : ***ADC Transfer to Digital Data bit9~bit0***

◆ **ADCON2**(0X143) : ***A/D Control Register #2***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADCON2	VREFS	-	-	-	-	ADCS2	ADCS1	ADCS0
R/W	R/W	-	-	-	-	R/W	R/W	R/W
RESET	0	-	-	-	-	0	0	0

VREFS : ***ADC Power Source Selection***

VREFS=0 , ADC Power Source use Internal LDO Output.

VREFS=1 , ADC Power Source use External power from PAD **PC0**.

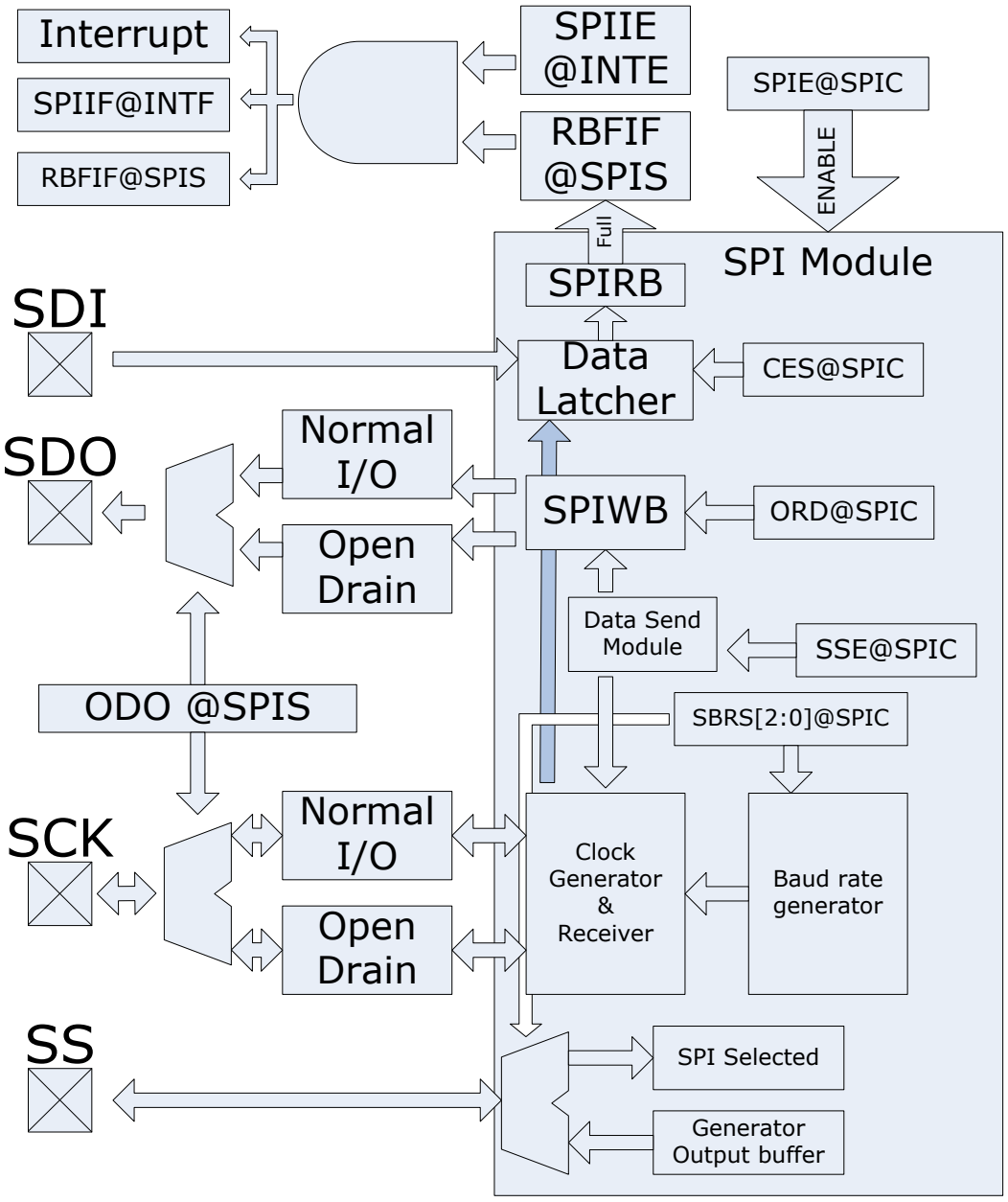
Note Input Power Voltage must be lower than 3.6V.

ADCS2~ADCS0 : ***ADC CLK Source:***

ADCS2	ADCS1	ADCS0	Clock (Hz)
0	0	0	Fosc/4
0	0	1	Fosc/8
0	1	0	Fosc/12
0	1	1	Fosc/16
1	0	0	Fosc/20
1	0	1	Fosc/24
1	1	0	Fosc/28
1	1	1	Fosc/32

14.0 SPI interface.

14.1 Overview



14.2 Registers

◆ **SPIC**(0X13D) : ***SPI Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIC	CES	SPIE	SRO	SSE	ORD	SBRS2	SBRS1	SBRS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	-	0	0	0	0

CES : *SPI Clock Edge Selection*

CES=0 , **Low go High** , Data Out; **High go Low** Data In.

CES=1 , **High go Low** , Data Out; **Low go High** Data In.

SPIE : *SPI Enable*

SPIE=0 ,SPI Disable.

SPIE=1 ,SPI Enable.

SRO : *Data In Overflow Flag (Only Used SLAVE Mode)*

SRO=1 ,Last Byte Data in SPI Read Buffer had not Read Out .

SRO=0 ,Otherwise.

SSE : *Start Shift SPI Data Out*

SSE=1 ,(a)Start Shift SPI Data Out.

(b) Completed Working , Clear SSE bit by Hardware .

SRO=0 ,Otherwise.

ORD : *SPI Data Shift Order*

ORD=0 ,MSB Bit First.

ORD=1 ,LSB Bit First.

SBRS2~SBRS0 : *SPI Baud Rate & Mode Selection*

SBRS2	SBRS1	SBRS0	Mode	Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Slave	SS Enable
1	1	0	Slave	SS Disable
1	1	1	Master	TMR1/2

◆ **SPIC2**(0X15D) : ***SPI-2 Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIC2	CES	SPIE	SRO	SSE	ORD	SBRS2	SBRS1	SBRS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	-	0	0	0	0

CES : *SPI Clock Edge Selection*

CES=0 , **Low go High** , Data Out; **High go Low** Data In.

CES=1 , **High go Low** , Data Out; **Low go High** Data In.

SPIE : *SPI Enable*

SPIE=0 ,SPI Disable.

SPIE=1 ,SPI Enable.

SRO : *Data In Overflow Flag (Only Used SLAVE Mode)*

SRO=1 ,Last Byte Data in SPI Read Buffer had not Read Out .

SRO=0 ,Otherwise.

SSE : *Start Shift SPI Data Out*

SSE=1 ,(a)Start Shift SPI Data Out.

(b) Completed Working , Clear SSE bit by Hardware .

SRO=0 ,Otherwise.

ORD : *SPI Data Shift Order*

ORD=0 ,MSB Bit First.

ORD=1 ,LSB Bit First.

SBRS2~SBRS0 : *SPI Baud Rate & Mode Selection*

SBRS~SBRS0 : ***Selection bits for Baud Rate & Mode***

SBRS	SBRS1	SBRS0	Mode	Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Slave	SS Enable
1	1	0	Slave	SS Disable
1	1	1	Master	TMR1/2

◆ **SPIS**(0X13C) : ***SPI Status Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIS	-	-	-	-	ODO	ODC	RBFIF	RBF
R/W-	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

ODO : ***SDO Open-Drain Control***

ODO=0 ,SDO Open-Drain Disable.

ODO=1 ,SDO Open-Drain Enable.

ODC : ***SCK Open-Drain Control***

ODC=0 ,SCK Open-Drain Disable.

ODC=1 ,SCK Open-Drain Enable.

RBFIF : ***SPI Read Buffer Full Interrupt Flag***

RBFIF=1 ,(a)Receive Completed, and Read Buffer is Full.
(b) Under the Interrupt Enable, and Interrupt Occur.

RBFIF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

RBFIF : ***SPI Read Buffer Full Flag***

RBF=1 ,Receive Completed, and Read Buffer is Full.

RBF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

◆ **SPIS2**(0X15C) : ***SPI-2 Status Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIS2	-	-	-	-	ODO	ODC	RBFIF	RBF
R/W-	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

ODO : ***SDO Open-Drain Control***

ODO=0 ,SDO Open-Drain Disable.

ODO=1 ,SDO Open-Drain Enable.

ODC : ***SCK Open-Drain Control***

ODC=0 ,SCK Open-Drain Disable.

ODC=1 ,SCK Open-Drain Enable.

RBFIF : ***SPI Read Buffer Full Interrupt Flag***

RBFIF=1 ,(a)Receive Completed, and Read Buffer is Full.

(b) Under the Interrupt Enable, and Interrupt Occur.

RBFIF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

RBFIF : ***SPI Read Buffer Full Flag***

RBF=1 ,Receive Completed, and Read Buffer is Full.

RBF=0 ,Receive Status is Ongoing , Read Buffer is Empty.

◆ **SPIRB**(0X13A) : ***SPI Data Read Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIRB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

◆ **SPIRB2**(0X15A) : ***SPI-2 Data Read Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIRB2	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

SPIRB/ SPIRB2 Register is a 8 bits Data Buffer for SPI Data Read In.

◆ **SPIWB**(0X13B) : ***SPI Data Write Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIWB	WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

◆ **SPIWB2**(0X15B) : ***SPI-2 Data Write Buffer***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPIWB2	WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

SPIWB/ SPIWB2 Register is a 8 bits Data Buffer for SPI Data Write Out.

◆ **INTE** (0x12F) : ***Hardware Interrupt Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTE	-	-	-	-	TR1IE	SPIIE	EXIE	TR0IE
R/W	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

SPIIE : *SPI Read Buffer Full Interrupt Enable*

SPIIE=0 , SPI Read Buffer Full Interrupt Disable .

SPIIE=1 , SPI Read Buffer Full Interrupt Enable .

◆ **INTF** (0x17F) : ***Interrupt Flag Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTF	-	-	-	-	TR1IF	SPIIF	EXIF	TR0IF
R/W	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

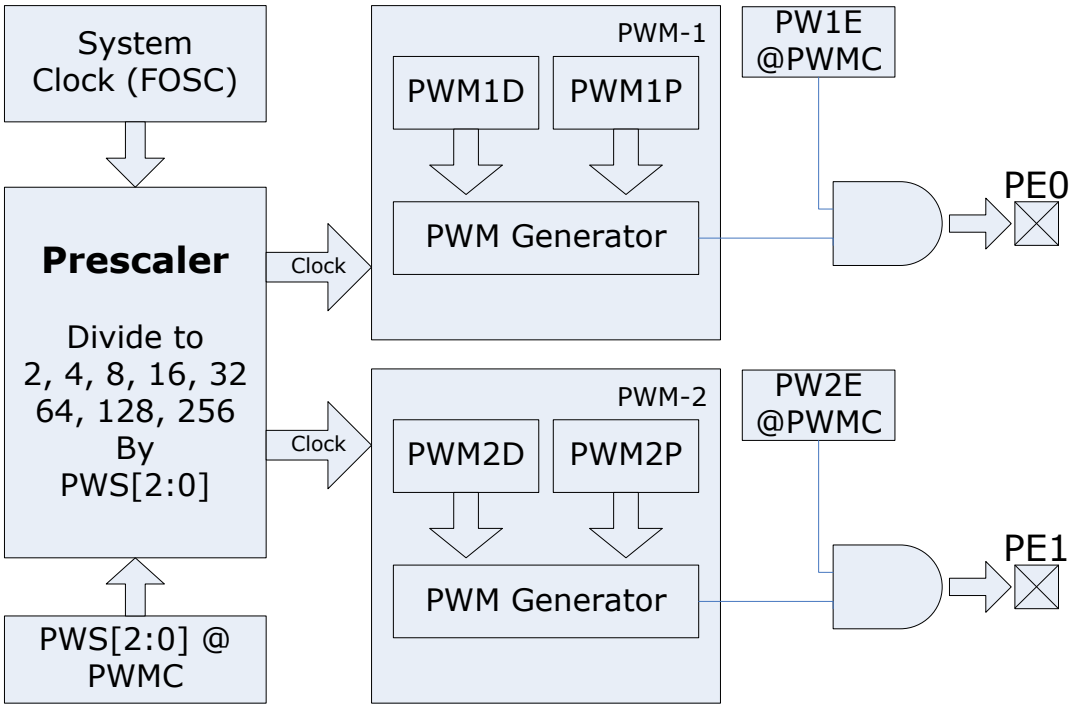
SPIIF : SPI Read Buffer Full Interrupt flag.

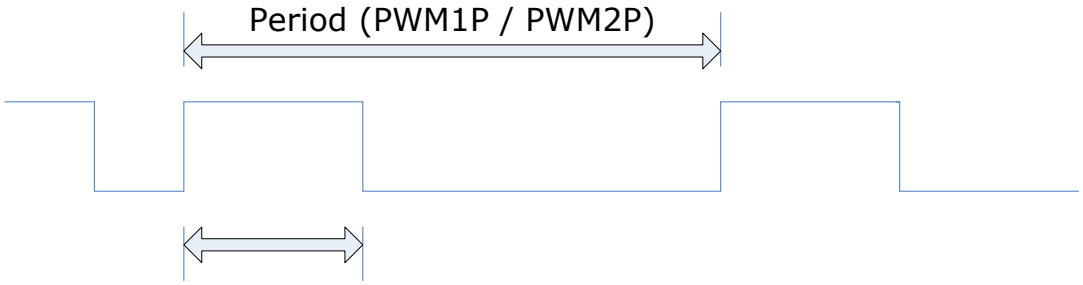
SPIIF = 0 , Clear it by Software.

SPIIF = 1 , When SPI read buffer full, this flag will be set to '1'.

15.0 PWM – Pulse Width Modulator.

15.1 Overview





Duty Cycle (PWM1D / PWM2D)

Duty Cycle = (PWMxD/PWMxP)*100%

15.2 Registers

◆ **PWMC** (0x134) : ***PWM Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWMC	PW2E	PW1E	-	-	-	PWS2	PWS1	PWS1
R/W	R/W	R/W	-	-	-	R/W	R/W	R/W
RESET	0	0	-	-	-	0	0	0

PW2E : *PWM2 Enable Bit*

PW2E=0 , PWM2 Disable.

PW2E=1 , PWM2 Enable.

PW1E : *PWM1 Enable Bit*

PW1E=0 , PWM1 Disable.

PW1E=1 , PWM1 Enable.

PWS2,PWS1,PWS0 : *PWM Clock Prescaler Rate*

PWS2	PWS1	PWS0	PWM Clock Rate
0	0	0	Fosc/2
0	0	1	Fosc/4
0	1	0	Fosc/8
0	1	1	Fosc/16
1	0	0	Fosc/32
1	0	1	Fosc/64
1	1	0	Fosc/128
1	1	1	Fosc/256

◆ **PWM1D** (0x130) : ***PWM1 Duty Cycle Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM1D	P1D7	P1D6	P1D5	P1D4	P1D3	P1D2	P1D1	P1D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P1D7~P1D0 : *8 bits PWM1 Duty Cycle Data*

◆ **PWM1P** (0x132) : ***PWM1 Period Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM1P	P1P7	P1P6	P1P5	P1P4	P1P3	P1P2	P1P1	P1P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P1P7~P1P0 : ***8 bits PWM1 Period Data***

Note: PWM1 Signal Output from PE0 PIN

◆ **PWM2D** (0x131) : ***PWM2 Duty Cycle Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM2D	P2D7	P2D6	P2D5	P2D4	P2D3	P2D2	P2D1	P2D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P2D7~P2D0 : ***8 bits PWM2 Duty Cycle Data***

◆ **PWM2P** (0x132) : ***PWM2 Period Data Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM2P	P2P7	P2P6	P2P5	P2P4	P2P3	P2P2	P2P1	P2P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W-	R/W-
RESET	0	0	0	0	0	0	0	0

P2P7~P2P0 : ***8 bits PWM2 Period Data***

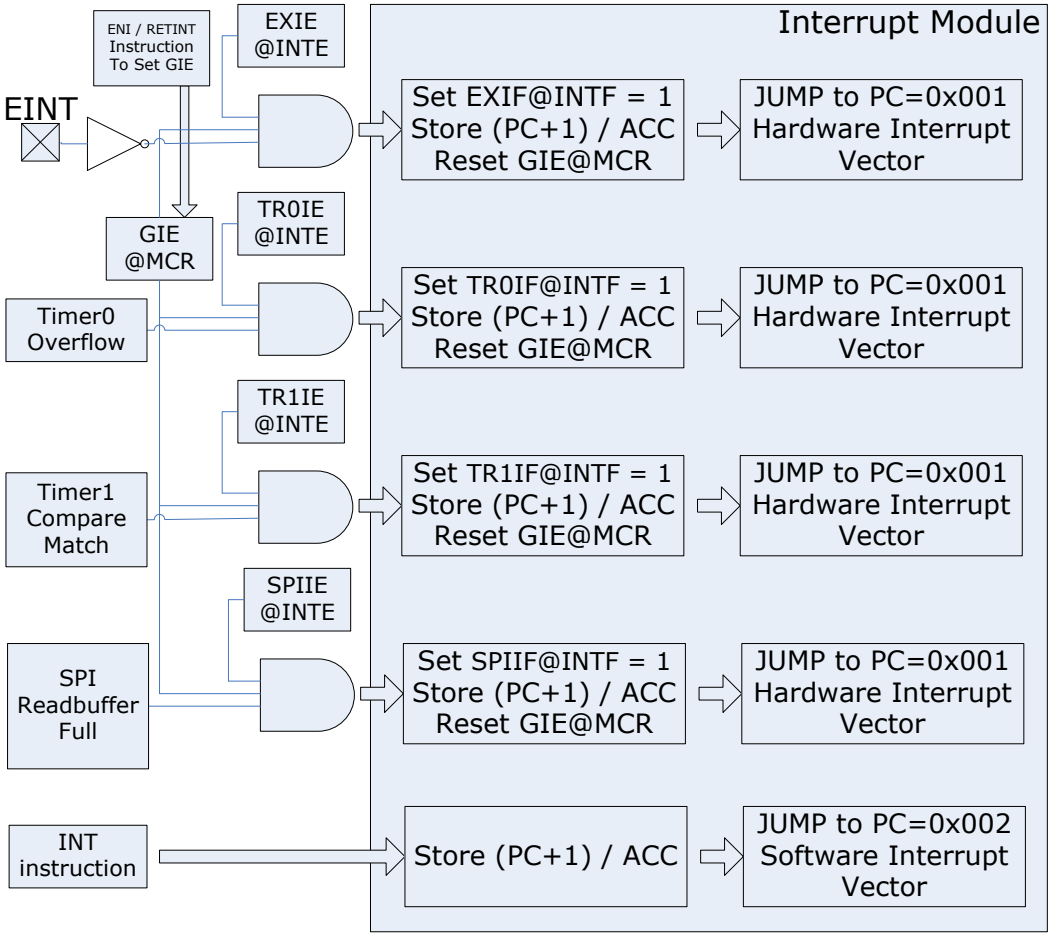
Note: PWM2 Signal Output from PE1 PIN

15.3 Code Setting Flow

```
MOV A,      @0X7F     ;Setup the PWM duty cycle register
MOV PWM1D,  A
MOV PWM2D,  A
MOV A,      @0XFF     ;Setup the PWM period data register
MOV PWM1P,  A
MOV PWM2P,  A
MOV A,      @0x02
MOV PWMC,   A         ; Set Prescaler to Fosc/8
BSR PWMC,   6         ; Active the PWM-1 module
BSR PWMC,   7         ; Active the PWM-2 module
;Now the PWM-1 and PWM-2 start to output the PWM signal.
```

16.0 Interrupts.

16.1 Overview



16.2 Registers

- **MCRW** (0x122) : ***Main Control Register for Write***
- **MCRR** (0x124) : ***Main Control Register for Read***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCRR	/PUE	GIE	-	-	PAB	PS2	PS1	PS0
R/W	R/W	R/W			R/W	R/W	R/W	R/W
RESET								

(Continue)

GIE : ***Global Interrupt Enable.***

GIE=0 Disable all interrupts. Execute DISI Instruction or accept Interrupt then GIE will be set to '0'. Reject any other Interrupt.

GIE=1 Global Enable all the Interrupt (Enable or not depend on others Register Enable Bit.
Execute ENI or RETI will be set to '1'. then accept others Interrupt.

◆ **INTE** (0x12F) : ***Hardware Interrupt Control Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTE	-	-	-	-	TR1IE	SPIIE	EXIE	TR0IE
R/W	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

SPIIE : *SPI Read Buffer Full Interrupt Enable*

SPIIE=0 , SPI Read Buffer Full Interrupt Disable .

SPIIE=1 , SPI Read Buffer Full Interrupt Enable .

◆ **INTF** (0x17F) : ***Interrupt Flag Register***

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTF	-	-	-	-	TR1IF	SPIIF	EXIF	TR0IF
R/W	-	-	-	-	R/W	R/W	R/W	R/W
RESET	-	-	-	-	0	0	0	0

SPIIF : SPI Read Buffer Full Interrupt flag.

SPIIF = 0 , Clear it by Software.

SPIIF = 1 , When SPI read buffer full, this flag will be set to '1'.

16.3 Instructions

ENI	*Enable Interrupt*
Operation	MCR/GIE Flag=0
Instruction Cycle	2
Affected Flag	None
Description	Enable Interrupt
Example	DISI

DISI	*Disable Interrupt*
Operation	MCR/GIE Flag=1
Instruction Cycle	2
Affected Flag	None
Description	Disable Interrupt
Example	DISI

INT	***Software Interrupt***
Operation	0001H --> PC, (PC+1) --> (Top Stack)
Instruction Cycle	4
Affected Flag	None
Description	Software Interrupt, go to 0001H Address(PC); Push the PC+1 to Top Stack
Example	ORG 0001H JMP SF_INT NOP SF_INT: NOP RETINT ; Feedback to LAB1 Main: NOP **INT** ; Software Interrupt ; go to 0001H Addr. LAB1 NOP ; ; Push LAB1 to Top Stack

RETINT	***Return from Interrupt.***
Operation	(Top Stack)--> PC, MCR/GIE Flag=1
Instruction Cycle	4
Affected Flag	None
Description	Return from Interrupt ; POP The Address from Top Stack
Example	ORG 0001H JMP SF_INT NOP SF_INT: NOP **RETINT** ; Feedback to LAB1 Main: NOP INT ; Software Interrupt ; go to 0001H Addr. LAB1 NOP ; ; Push LAB1 to Top Stack

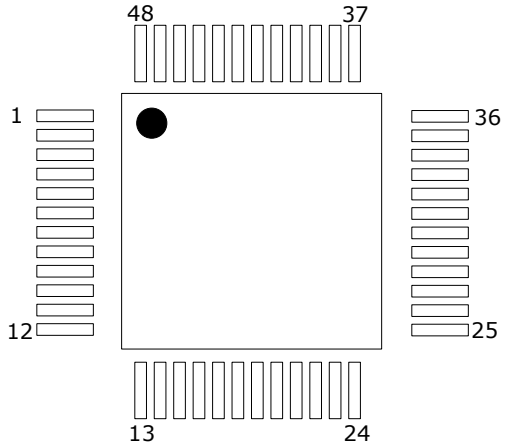
17.0 Electrical Characteristics.

17.1 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VOP	Operating Voltage	LDO ON	2.2		5.0	V
IOP	Operating current			2		mA
ISB	Standby current			1		uA
FXTL	XTAL frequency				16	MHz
FIRC	Internal RC Frequency				16	MHz
IIH	Internal Pull-Low current			30		uA
IIL	Internal Pull-High current			40		uA
IOH	Output High current			7		mA
IOL	Output low current			14		mA

Appendix.1 Package Information.

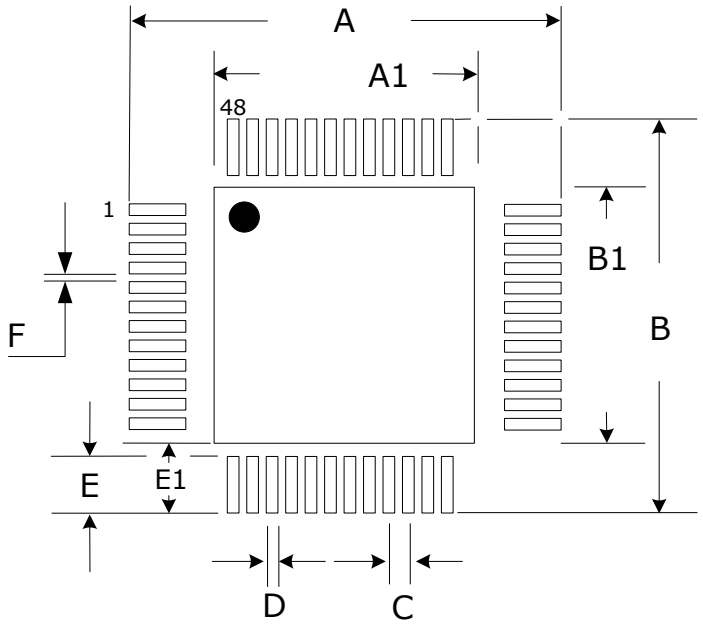
A1.1 LQFP48



Pin Definition

Pin	NAME	Pin	NAME	Pin	NAME
1	PD7/AD15	17	PB0	33	PF2
2	PA0/AD0	18	PB1	34	EINT/PF3
3	PA1/AD1	19	PB2/SDI2	35	PF4/VPP
4	PA2/AD2	20	PB3/SDO2	36	RSTN/PF5
5	PA3/AD3	21	PB4/SCK2	37	VDD
6	PA4/AD4	22	PB5/SS2	38	VDDL
7	PA5/AD5	23	PB6/TX	39	OSCI/PF6
8	PA6/AD6	24	PB7/RX	40	OSCO/PF7
9	PA7/AD7	25	PE0/PWM1	41	VSS
10	PC0/VREF	26	PE1/PWM2	42	PD0/AD8
11	PC1	27	PE2/SDI1	43	PD1/AD9
12	PC2	28	PE3/SDO1	44	PD2/AD10
13	PC3	29	PE4/SCK1	45	PD3/AD11
14	PC4	30	PE5/SS1	46	PD4/AD12
15	PC5	31	PF0	47	PD5/AD13
16	VSS	32	PF1	48	PD6/AD14/DAC

Package Dimension



Symbol	Min	Typ.	Max.
A		9.0 BSC	
A1		7.0 BSC	
B		9.0 BSC	
B1		7.0 BSC	
C		0.5 BSC	
D	0.17	0.22	0.27
E	0.45	0.6	0.75
E1		1.0 REF	
F	0.23	0.28	0.33

All dimensions shown in MM.

Appendix.2 Programming Information.

A2.1 Programming Pins

Pin	Name	Write Pin	Writer-48	Writer-20	Notes
2	PA0/AD0	CS	13	19	
3	PA1/AD1	DIO1	38	2	
4	PA2/AD2	DIO2	39	3	
5	PA3/AD3	SCK	12	18	
-	-	RST	11	4	
37	VDD	VDD	14	20	
38	VDDL	VDD			
36	RSTN/PF5	VSS	11	4	
41	VSS	VSS			
35	PF4/VPP	VPP	37	1	

Notes.

Writer-48 : The DIP48 slot on the writer.

Writer-20 : The Wide-20 pins slot on the writer.

Appendix.3 Support Information.

A If you need any support or suggestions, there are support method which you can contact with:

E-Mail :
mcu.support@ystek.com.tw
Telephone :
+886-3-5739389(Taiwan) call for MCU.FAE Support.
Websites :
http://www.ystek.com.tw