Feature

- Built-in 8bit CPU (Mini-Jupiter(A)) micro processor.
- Internal system and CPU clock 18 MHz (Typical).
- DH98020 Internal 512Kbit (64 K Bytes) OTP memory, for program code or audio data.
- Internal 2Kbit(256 Bytes) SRAM for working memory.
- Internal R/C (Base-Clock) and DPLL(Programmable PLL Clock) .
- Features 32768 XTAL interface.
- Features one OP amplifier for signal filter or integrator.
- Features one 16bit D/A for audio output.
- Features one 12bit PWM for audio output.
- Internal two 8bit Timer (Timer-0 and Timer-1).
- Features 12 general purpose I/O and port 0 supports external triggering wake-up.
- Features Low Voltage Reset circuit (LVR).
- 8-polyphonic software MIDI instructions.
- Internal Watch-Dog Timer circuit (WDT).
- Features one Class AB/PWM speaker amplifier 8 /0.25W.
- Operating voltage (2.4V~3.6V).
- Standby current (Power Down): 2uA.

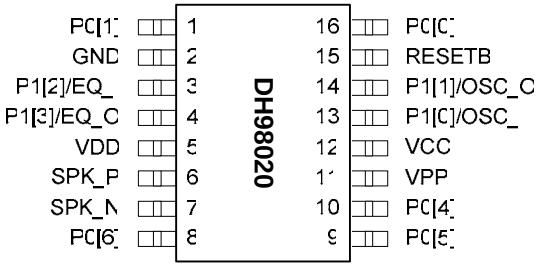
Description

The DH98020 is based on OTP memory for voice controller. With high performance 8-bit CPU core, it can be designed to many application fields by software.

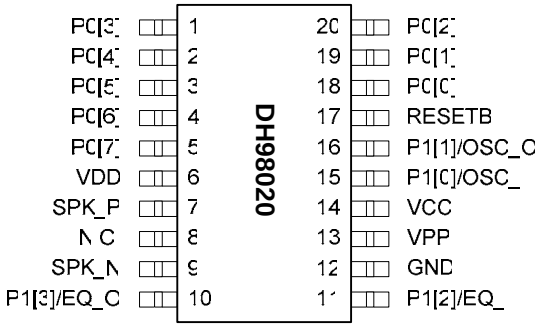
Features the powerful class-A/B speaker amplifier and Delta-Sigma DAC, it can provides good quality audio/voice Outputting. There is one optional set of external clock for 32768Hz crystal.

Helios provides the IDE (Integrated development system) for programming assembly language and the easy statement function for simply speech application.

Pin Configuration



SOP-16 (150mil)



SOP-20 (300mil)

DC Characteristics (V_{CC} = 3.0V, V_{DD} = 3.0V, GND = 0V, TA = 25℃)

Symbol	Parameter	Min.	Type.	Max.	Unit	Condition
PORT0	Driving Current		4		mA	V_{OH}=2.7
PORT1	Driving Current		0.5		mA	V_{OH}=2.7
OP_O	Driving Current		4		mA	
SPK_P SPK_N	Driving Current			300	mA	R_L=8
PORT0	Sink Current		4		mA	V_{OL}=0.3
PORT1	Sink Current		1		mA	V_{OL}=0.3
OP_O	Sink Current		4		mA	
SPK_P SPK_N	Sink Current			300	mA	R_L=8
I_STD	Standby Current	0.5	1	2	uA	
Play Speech	Applicatipn Current	11	53		mA	R_L=8
	RTC Current	7.6			uA	

Pin Definition

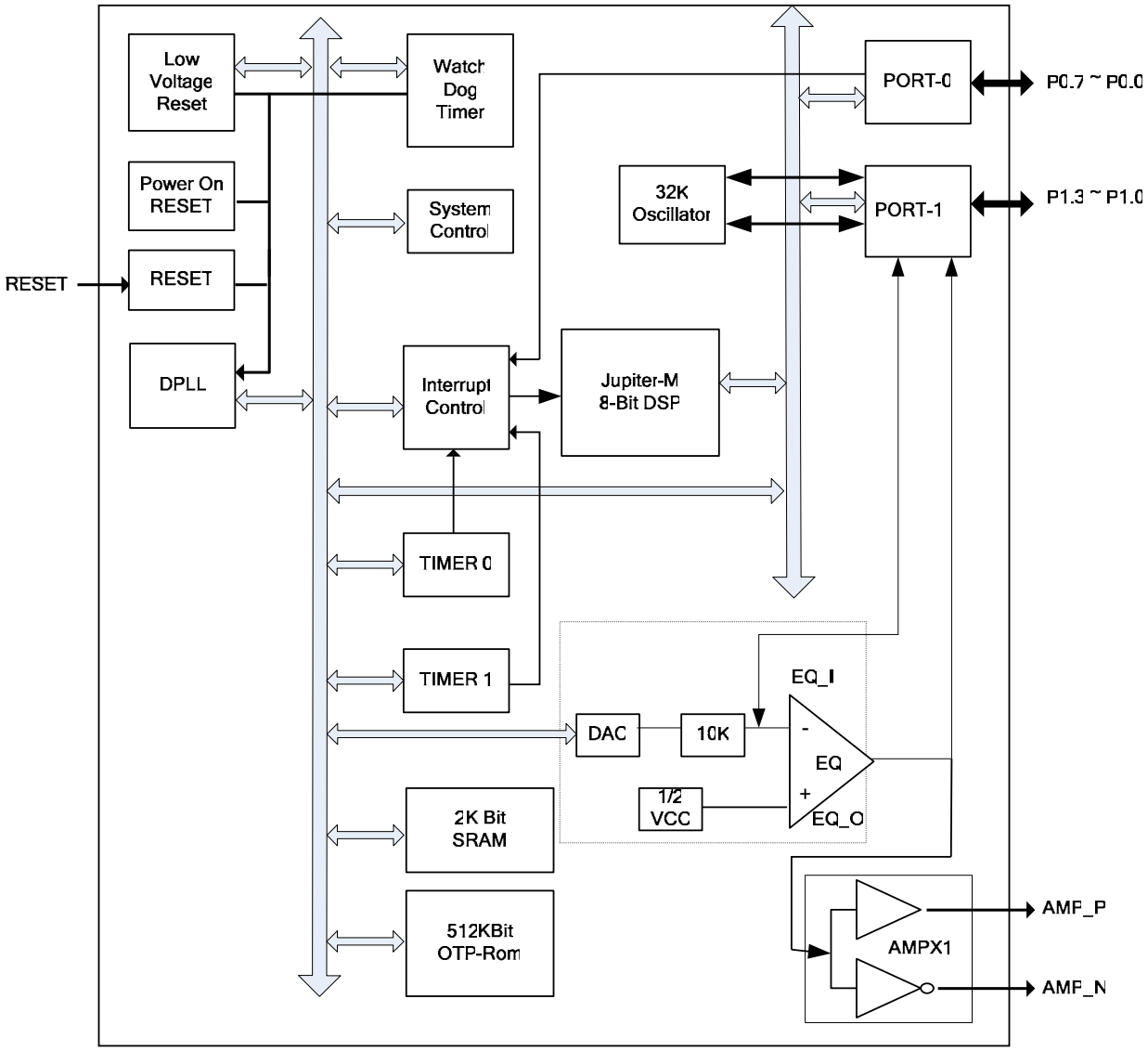
SOP 16

Pin No.	Designation	I/O	SMT	Description
1	P0[1]	I/O	S	Port-0 I/O Bit1.
2	GND	P		System Ground
3	P1[2]/EQ_I	I/O		Port-1 I/O Bit2.Equalizer Input
4	P1[3]/EQ_O	I/O		Port-1 I/O Bit3.Equalizer Output
5	V_{DD}	P		Analog Power
6	SPK_P	O		Speak Out Port
7	SPK_N	O		Speak Out Port
8	P0[6]	I/O	S	Port-0 I/O Bit6.
9	P0[5]	I/O	S	Port-0 I/O Bit5.
10	P0[4]	I/O	S	Port-0 I/O Bit4.
11	V_{PP}	P		OTP Programming Power
12	V_{CC}	P		Digital Power
13	P1[0]/OSC_I	I/O		Port-1 I/O Bit0.Oscillate Input.
14	P1[1]/OSC_O	I/O		Port-1 I/O Bit1.Oscillate Output
15	RESETB	I	S	System Reset.
16	P0[0]	I/O	S	Port-0 I/O Bit0.

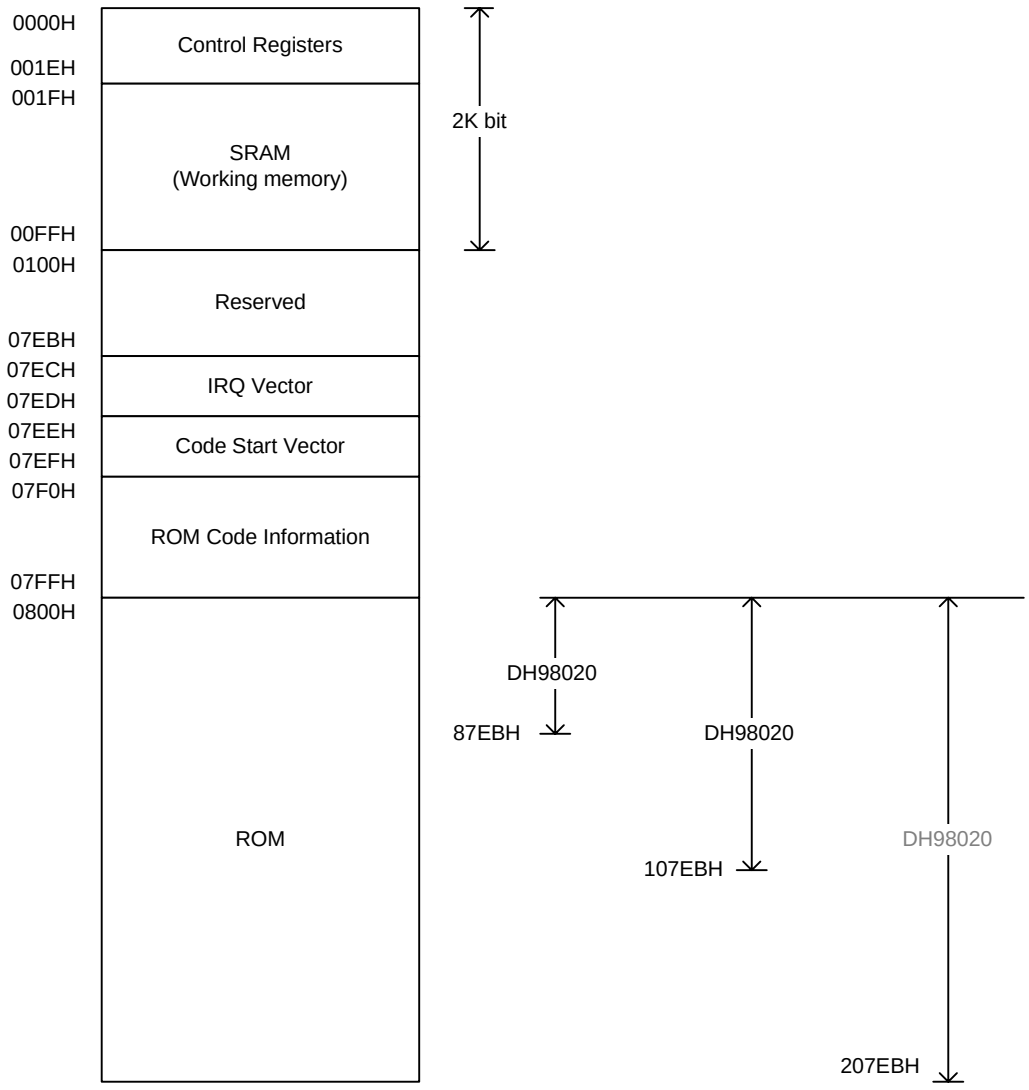
SOP 20

Pin No.	Designation	I/O	SMT	Description
1	P0[3]	I/O	S	Port-0 I/O Bit3.
2	P0[4]	I/O	S	Port-0 I/O Bit4.
3	P0[5]	I/O	S	Port-0 I/O Bit5.
4	P0[6]	I/O	S	Port-0 I/O Bit6.
5	P0[7]	I/O	S	Port-0 I/O Bit7.
6	V_{DD}	P		Analog Power
7	SPK_P	O		Speak Out Port
8	NC			NO Connect
9	SPK_N	O		Speak Out Port
10	P1[3]/EQ_O	I/O		Port-1 I/O Bit3.Equalizer Output
11	P1[2]/EQ_I	I/O		Port-1 I/O Bit2.Equalizer Input
12	GND	P		System Ground
13	V_{PP}	P		OTP Programming Power
14	V_{CC}	P		Digital Power
15	P1[0]/OSC_I	I/O		Port-1 I/O Bit0.Oscillate Input.
16	P1[1]/OSC_O	I/O		Port-1 I/O Bit1.Oscillate Output
17	RESETB	I	S	System Reset.
18	P0[0]	I/O	S	Port-0 I/O Bit0.
19	P0[1]	I/O	S	Port-0 I/O Bit1.
20	P0[2]	I/O	S	Port-0 I/O Bit2.

Block Diagram



Memory Map



000000H – 00001EH : System control registers.
00001FH – 0000FFH : SRAM for working memory.
000800H – 0087EBH : DH98020 OTP for program or data.
000800H – 0107EBH : DH98020 OTP for program or data.
000800H – 0207EBH : DH98020 OTP for program or data.

Control Registers Table

Address (Hex)	Simplified Name	Complete Name	Register Function Brief
0000	SCR	System Control Register	System clock on/off, Equalizer EQ's on/off, Speaker Amplifier on/off, DAC output mode on/off, RTC on/off
0001	IRQER	Interrupt Request Enable Register	Interrupt control register, enable/disable TIMER0/TIMER1/PORT0/PWM interrupts
0002	IRQSR	Interrupt Status Register	Interrupt Status, to indicate the status of TIMER0/TIMER1/PORT0/PWM interrupts
0003	PWMR	PWM Register	Configure PWM Over-Sampling Interrupt, DAC signed/unsigned
0004 0005	DACR	DAC Register	16-bit DAC output control register
0006	TMR	Timer Control Register	Timer 0/1 counters enable/disable, pre-scale clock select.
0007	T0RR	Timer 0 Reload Register	Set timer 0 counter reload value.
0008	T0DR	Timer 0 Data Register	Set timer 0 counter values or get timer 0 current count values.
0009	T1RR	Timer 1 Reload Register	Set timer 1 counter reload value.
000A	T1DR	Timer 1 Data Register	Set timer 1 counter value or get timer 1 current count value.
000B	P0IMR	Port 0 Interrupt Mask Register	Enable/disable each port 0 input interrupt source.
000C	P0IPR	Port 0 Interrupt Polarity Register	Select interrupt trigger condition, falling or rising edge.
000D	P0ISR	Port 0 Interrupt Status Register	Indicate the port 0 interrupt assert or not.
000E	P0MR	Port 0 I/O Mode Register	Set the port 0 I/O direction.
000F	P0PR	Port 0 Pull-up Control Register	Select port 0 I/O pull-up register or not.
0010	P0DR	Port 0 Data Register	Set the port 0 output data, or get the port 0 pin logical.
0011	P1MR	Port 1 I/O Mode Register	Set the port 1 I/O direction.
0012	P1PR	Port 1 Pull-up Control Register	Select port 1 I/O pull-up register or not.
0013	P1DR	Port1 Data Register	Set the port 1 output data, or get the port 0 pin logical.
0018	WDTC	Watch Dog Control Register	SET/Clear the Watch Dog Timer
0019	ACR	Advance Control Register	SET CPU Clock divider, Timer-1 Output on/off , LVR on/off
001A 001B 001C	PTRAR	PTR Access Register	the 24 bits register to access the memory data by read PTR_DATA
001D	PTRDR	PTR Data Register	
001E	DPLLR	DPLL Control Register	Configure for system clock.

0000H: System Control Register (SCR)

0000H , System Control Register (SCR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Clock On/Off	Select System Clock	32768 XTAL on/off	Select Low Clock	Speaker Amplifier On/Off	DAC Output Mode		EQ-OP On/Off
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

D [0] EQ Enable/Disable, default 0:
- 0 = Disable.
- 1 = Enable.

Set this bit to 1 for enabling the EQ-OP and the PORT1[2] is switched to EQ_I, PORT1[3] is switched to EQ_O.

D [2:1] Select the Speaker Amplifier (AMP) mode, default 0:
- 0 = Reserved.
- 1 = PWM mode.
- 2 = Analog mode (Class-AB mode).
- 3 = Digital-Drive Power Down.

This function is SPK which makes the sound channel about _ P and SPK _ N urges by imitating signal urging or digit signal. If it is 2 to set up, it is EQ to imitate the signal source _ LI and EQ _ the signal of receiving the foot of RI is a basis. If set up as 1, the signal source of PWM is an basis that link within the system, it is that the number value of consulting DAC determines work period that PWM outputs the signal, act as and set as 0 or 3, and AMP is under the state of Enable, SPK _ It is GND and SPK that N is regular P is the high impedance . When Power Down , Port1 need PULL HIGH.

AMP Enable D[3]	AMP Mode D[2:1]	SPK_N	SPK_P	Mode
0	1 0	Floating	GND	DAC Enable
0	0 1	Floating	GND	PWM Enable
0	0 0, 1 1	Floating	GND	
1	1 0	Analog	Analog	Class A/B
1	0 1	Duty	Duty	PWM
1	0 0, 11	GND	GND	Power Down

D [3] Enable/Disable Speaker Amplifier (AMP), default 0:
- 0 = Disable.
- 1 = Enable.

When enable, refer to the mode setting for driving the SPK_P and SPK_N.
When disable, the SPK_P and SPK_N are both floating.

D[4] Select Low Clock , default 0:
- 0 = Select R/C (Base Clock, H5A021P: 2MHz ,H5A02HP: 1.85MHz, H5A02QP: 2MHz).
- 1 = Select 32768 XTAL.

D[5] 32768 XTAL on/off, default 0:
- 0 = Off.
- 1 = On.

The connect pins of 32768 XTAL are OSC_I and OSC_O that are optional with PORT1[0] and PORT1[1] by OTP programming time. Therefore, using the Helios tools to select this function.

D[6] Select System Clock, default 0:
- 0 = Select low clock, R/C or 32768.
- 1 = Select high clock, PLL (24 MHz).

D[7] R/C Clock on/off, default 1:
- 0 = Off.
- 1 = On.

CPU Clock	System Control			
	D[7]	D[6]	D[5]	D[4]
Power Down	0	1	X	X
32768 Hz	0	0	1	1
R/C Clock	1	0	X	0
High Clock	1	1	X	X

Notice:

1.When theDH98020 is wake up from the power down mode, only the R/C (base clock) works, so the D[4] must be 0 before the system entering the power down mode.
2. Must write DPLL Control and write System again _ Control, will just carry out Delay 1ms.
3. Avoid at the same time switching over D [5] of D [6] (Hi Low Clock) Will hang and lose or to close at the same time unstably.
4. While entering Powerdown under 32K, need to remove the state of cutting off, otherwise will be woken up.

Interrupts

There are 4 interrupt sources in DH98020:

- Timer0 Interrupt
- Timer1 Interrupt
- Port-0 Interrupt
- PWM Interrupt

0001H: Interrupt Request Enable Register(IRQER)

0001H , Interrupt Request Enable Register(IRQER)								
Bit No.	7	6	5	4	3	2	1	0
Bit Name					PWM IRQ ON/OFF	Port-0 IRQ ON/OFF	Timer-1 ON/OFF	Timer-0 ON/OFF
Read/Write					R/W	R/W	R/W	R/W
Reset					0	0	0	0

D[0] Timer-0 IRQ Enable/Disable:
D[1] Timer-1 IRQ Enable/Disable:
D[2] Port-0 IRQ Enable/Disable:
D[3] PWM IRQ Enable/Disable:

- 0 = Disable.
- 1 = Enable.

0002H: Interrupt Status Register(IRQSR)

0002H , Interrupt Status Register(IRQSR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name					PWM IRQ Unaffect /Clear	Port-0 IRQ Unaffect /Clear	Timer-1 Unaffect /Clear	Timer-0 Unaffect /Clear
Read/Write					R/W	R/W	R/W	R/W
Reset					0	0	0	0

D[0] Timer-0 Interrupt Status.
D[1] Timer-1 Interrupt Status.
D[2] Port-0 Interrupt Status.
D[3] PWM Interrupt Status.

Read the status bit:

- 0 = No interrupt.
- 1 = Interrupt assert.

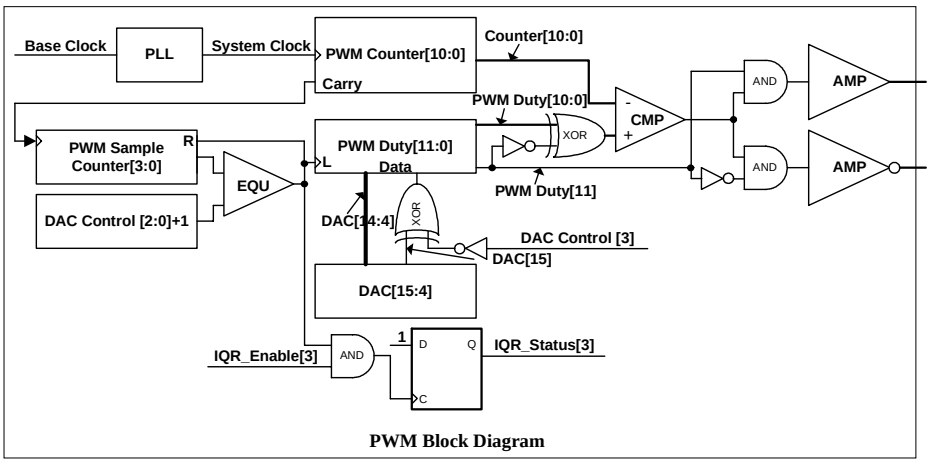
Write the status bit

- 0 = Clear the status (EOI, End of Interrupt).
- 1 = Unaffected.

Notice : The bit 2 (Port-0 interrupt status) can't be cleared directly, only all the bits(8-bits) of PORT0_IRQ_STATS(address 000DH) are all 0 (or be cleared to 0), the bit 2 of this register is 0, in other words, the bit 2 of IRQ_STATUS is the logical-OR form the 8 bits of PORT0_IRQ_STATUS.

0003H:PWM Register(PWMR)

0003H , PWM Register(PWMR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name					DAC signed/unsigned	Configure PWM Over-Sampling Interrupt		
Read/Write					R/W	R/W	R/W	R/W
Reset					0	0	0	0



PWM Block Diagram

D[2:0] Configure PWM Over-Sampling Interrupt, default 0:
Over-Sampling = (D[2:0] + 1)
The PWM update the DAC data in period of Over-Sampling, then asserts the interrupt status.
The PWM is 11-bit resolution (2048 duty cycle) and 1-bit(MSB) signed to output on SPK_P or SPK_N.

D[3] DAC signed/unsigned, default 0:
- 0 = Unsigned.
- 1 = Signed.

0004H, 0005H:DAC Register(DACR)

0004H ,0005H,DAC Register(DACR)																
	0004H High Byte							**0005H Low Byte**								
Bit No.	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	**16-bit Left DAC Data**															
Read/Write	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Reset	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

16-bit DAC data register.
Write low byte will be latched temporary and not affect the DAC output, and write high byte will update the DAC output.

0006H: Timer Control Register(TMR)

0006H ,Timer Mode Register (TMR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Timer 1 Count Enable	Timer 1 Clock Source select	Timer 1 clock pre-scale		Timer 0 Count Enable	Timer 0 clock pre-scale		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D[2:0] Select the clock of Timer-0:
- 0 = CPU Clock.
- 1 = CPU Clock / 4.
- 2 = CPU Clock / 16.
- 3 = CPU Clock / 64.
- 4 = CPU Clock / 256.
- 5 = CPU Clock / 1024.
- 6 = CPU Clock / 4096.
- 7 = CPU Clock / 16384.

D[3] Timer-0 Enable/Disable:

■ 0= Disable.
■ 1= Enable.

D[5:4] Select the source clock of Timer-1:
■ 0 = Clock.
■ 1 = Clock / 8.
■ 2 = Clock / 64.
■ 3 = Clock / 1024.

D[6] Select the source clock of Timer-1:
■ 0 = Low Clock (R/C or 32768 Hz，selected by bit 4 of SYSTEM_CONTROL).
■ 1 = CPU Clock.

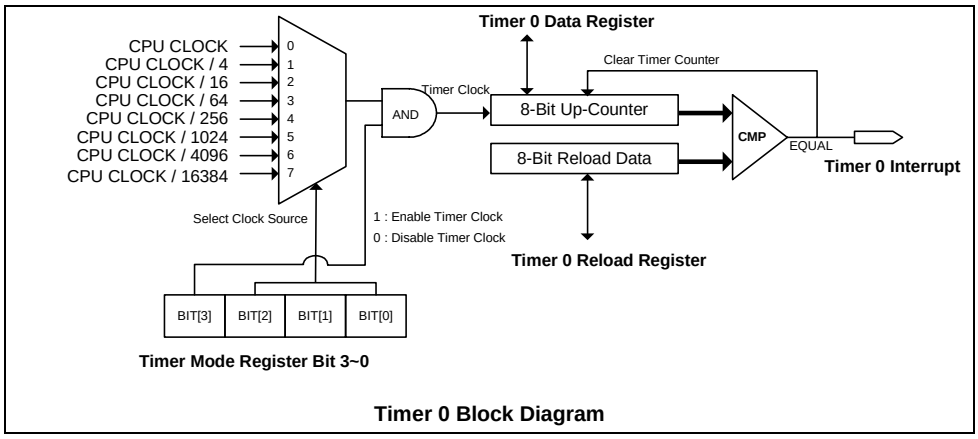
D[7] Timer-1 Enable/Disable:
■ 0 = Disable.
■ 1 = Enable.

Notice:

When the timer 1 is switched between different clock sources, make sure to wait for more than 5 instruction cycles between the clock switching.

Especially, when Timer1 Clock Source is selected to 32k from Base Clock, the waiting procedure is necessary.

Timer0



Timer 0 Block Diagram

0007H: Timer 0 Reload Register(T0RR)

0007H , Timer 0 Reload Register (T0RR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Timer 0 counter reload value							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

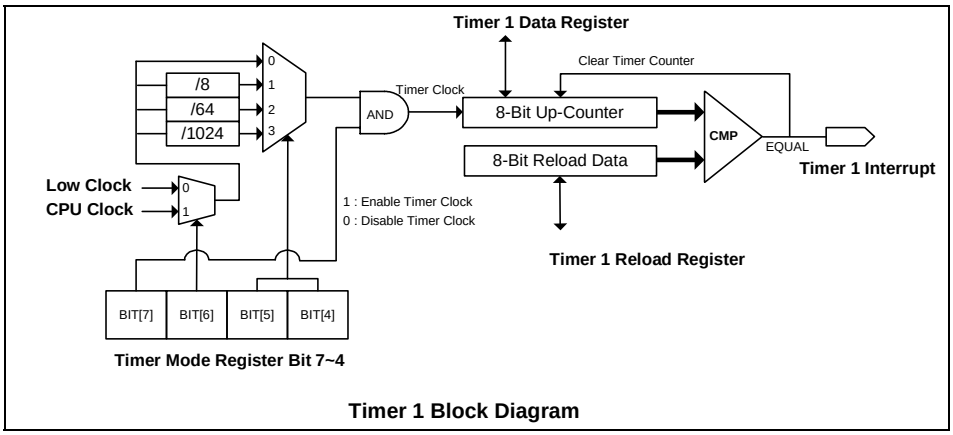
Set the compared value of Timer-0, Timer-0 and Timer-1are both up-counters.
The timer 0 counter will be reset to 0 while the counter value is equal to the reload value (also called compare value), and then, the timer 0 interrupt status will be set 1.
The default value is FFH.

0008H: Timer 0 Data Register (T0DR)

0008H , Timer 0 Data Register (T0DR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Timer 0 Counter Value							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Timer-0 counter value. default 00H.

Timer1



Timer 1 Block Diagram

0009H: Timer 1 Reload Register(T1RR)

0009H , Timer 1 Reload Register (T1RR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Timer 1 counter reload value							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

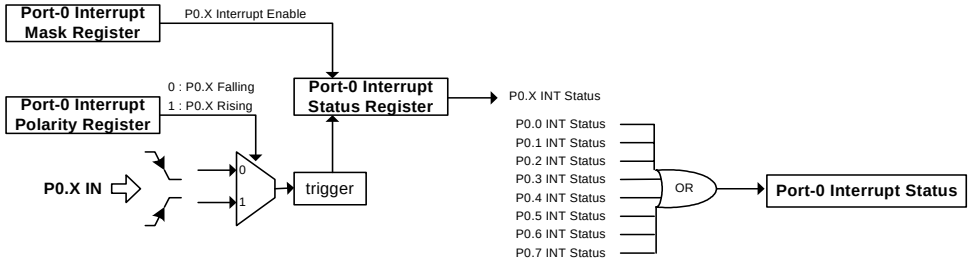
Set the compared value of Timer-1. default FFH.

000AH:Timer 1 Data Register(T1DR)

000AH , Timer 1 Data Register (T1DR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Timer 1 Counter Value							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Timer-1 counter value. default 00H.

Port-0 IRQ



Port-0 Interrupt Function Diagram

000BH : Port 0 Interrupt Mask Register(P0IMR)

000BH , Port-0 Interrupt Mask Register (P0IMR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	PORT0[7] Interrupt Enable/Disable	PORT0[6] Interrupt Enable/Disable	PORT0[5] Interrupt Enable/Disable	PORT0[4] Interrupt Enable/Disable	PORT0[3] Interrupt Enable/Disable	PORT0[2] Interrupt Enable/Disable	PORT0[1] Interrupt Enable/Disable	PORT0[0] Interrupt Enable/Disable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Enable or disable the external interrupt source of Port-0. default 00H.

- 0 = Disable.
- 1 = Enable.

000CH: Port 0 Interrupt Polarity Register(P0IPR)

000CH , Port-0 Interrupt Polarity Register (P0IPR)

Bit No.	7	6	5	4	3	2	1	0
Bit Name	PORT0[7] Interrupt Polarity	PORT0[6] Interrupt Polarity	PORT0[5] Interrupt Polarity	PORT0[4] Interrupt Polarity	PORT0[3] Interrupt Polarity	PORT0[2] Interrupt Polarity	PORT0[1] Interrupt Polarity	PORT0[0] Interrupt Polarity
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

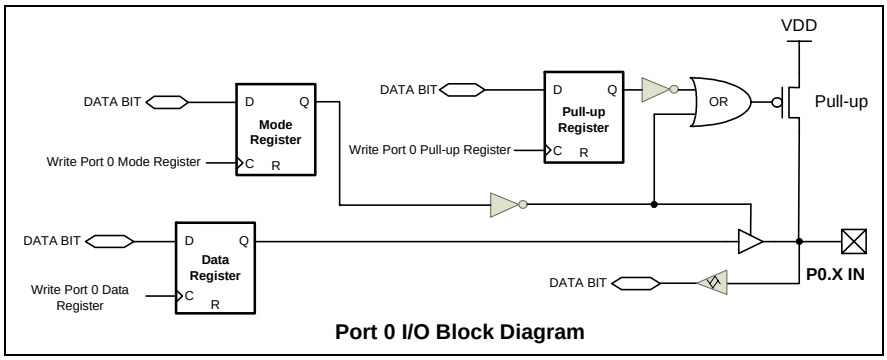
Set polarity of external interrupt. default 00H.

- 0 = Falling polarity (falling edge).
- 1 = Rising polarity (rising edge).

000DH : Port 0 Interrupt Status Register(P0ISR)

000DH , Port-0 Interrupt Status Register (P0ISR)								
Bit No.	7	6	5	4	3	2	1	0
Bit Name	PORT0[7] Interrupt Status	PORT0[6] Interrupt Status	PORT0[5] Interrupt Status	PORT0[4] Interrupt Status	PORT0[3] Interrupt Status	PORT0[2] Interrupt Status	PORT0[1] Interrupt Status	PORT0[0] Interrupt Status
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Read this status bits to indicate which external interrupt assert. Write 0 to the status for clearing the interrupt status, also called EOI(End of interrupt by controller), in the other, write 1 will not affect the status bit.



Port 0 I/O Block Diagram

000EH : Port 0 I/O Mode Register(P0MR)

000EH , Port 0 I/O Mode Register (P0MR)								
Bit No.	7	6	5	4	3	2	1	0
Bit Name	PORT0[7] Input/Output Select	PORT0[6] Input/Output Select	PORT0[5] Input/Output Select	PORT0[4] Input/Output Select	PORT0[3] Input/Output Select	PORT0[2] Input/Output Select	PORT0[1] Input/Output Select	PORT0[0] Input/Output Select
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Port-0 input mode or output mode. default FFH(all input mode).

- 0 = Output mode.
- 1 = Input mode.

00FH: Port 0 Pull-up Control Register (P0PR)

000FH , Port 0 Pull-up Register (P0PR)								
Bit No.	7	6	5	4	3	2	1	0
Bit Name	PORT0[7] Pull-up Enable	PORT0[6] Pull-up Enable	PORT0[5] Pull-up Enable	PORT0[4] Pull-up Enable	PORT0[3] Pull-up Enable	PORT0[2] Pull-up Enable	PORT0[1] Pull-up Enable	PORT0[0] Pull-up Enable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

default FFH.

To enable the pull-up resistors of corresponding pins of Port-0 (each about 10kOhm). default FFH.

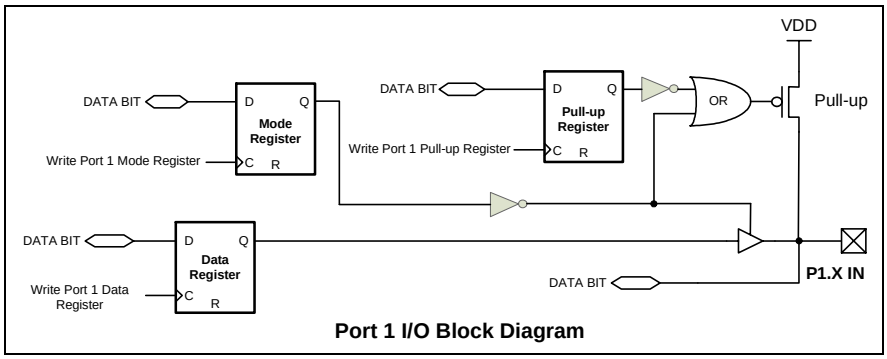
- 0 = Pull-up Disable.
- 1 = Pull-up Enable.

0010H: Port 0 Data Register (P0DR)

0010H , Port 0 Data Register (P0DR)								
Bit No.	7	6	5	4	3	2	1	0
Bit Name	PORT0[7] Data Bit	PORT0[6] Data Bit	PORT0[5] Data Bit	PORT0[4] Data Bit	PORT0[3] Data Bit	PORT0[2] Data Bit	PORT0[1] Data Bit	PORT0[0] Data Bit

Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Write this register to control the port 0output.
Read this register to get the input level (direct from pin, not register value).
Notice: There are Schmitt-Triggers on the input of port 0, refer to the block diagram.



Port 1 I/O Block Diagram

0011H: Port 1 I/O Mode Register (P1MR)

0011H , Port 1 I/O Mode Register (P0MR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	PORT1[7] Input/Output Select	PORT1[6] Input/Output Select	PORT1[5] Input/Output Select	PORT1[4] Input/Output Select	PORT1[3] Input/Output Select	PORT1[2] Input/Output Select	PORT1[1] Input/Output Select	PORT1[0] Input/Output Select
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Port-1Input/Output mode. default FFH.
- 0 = Output.
- 1 = Input.

0012H:Port 1 Pull-up Control Register(P1PR)

0012H , Port 1 Pull-up Register (P1PR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	PORT1[7] Pull-up Enable	PORT1[6] Pull-up Enable	PORT1[5] Pull-up Enable	PORT1[4] Pull-up Enable	PORT1[3] Pull-up Enable	PORT1[2] Pull-up Enable	PORT1[1] Pull-up Enable	PORT1[0] Pull-up Enable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Default 00H.
- 0 = Pull-up Disable.
- 1 = Pull-up Enable.

Set 1 to the bits for enabling the corresponding pull-up resistor(about 10K Ohm). default is 00H(Notice : Port-0 Pull-up control default is FFH).
If the corresponding pin is configured to output mode, the pull-up setting will disable the pull-up.

0013H:Port1 Data Register(P1DR)

0013H , Port 1 Data Register (P1DR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	PORT1[7] Data Bit	PORT1[6] Data Bit	PORT1[5] Data Bit	PORT1[4] Data Bit	PORT1[3] Data Bit	PORT1[2] Data Bit	PORT1[1] Data Bit	PORT1[0] Data Bit
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	1

Write this register to control the port 1 output.
Read this register to get the input level(direct from pin, not register value).

0018H: Watch Dog Control Register(WDTC)

0018H , Watch Dog Control Register(WDTC)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Configure the watch-dog-timer				Clear			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D[3:0] Control Watch-Dog-Timer(WDT):

05H = Clear.
Write 05H to this register for clearing the watch-dog-timer.

D[7:4] Configure the watch-dog-timer period, default 0:
The clock of Watch-Dog-Timer is Base-Clock / (15-D[7:4]+1), if this timer (15-bit timer counter) is overflow, the system is reset.
The default timer period is 262.144 mS after reset CPU.

0019H:Advance Control Register(ACR)

0019H , Advance Control Register(ACR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name					LVR ON/OFF	Timer-1 Out DUTY ON/OFF	CPU Clock divider	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	1	0	0	0

D[1:0] CPU Clock divider, default 00:
The clock of CPU (mini-jupiter (A)) is configured to DPLL -Clock / (D[1:0]+2).

D[2] Timer-1 Output enable/disable, default 0:
- 0 = Disable.
- 1 = Enable.

Set this bit 1 to enable Timer-1output on PORT0[7], and this output is a square wave form in 50% duty
To program the timer 1 to generate the frequency of this output signal.

D[3] Low Voltage Reset (LVR), default 1.
- 0 = Disable .
- 1 = Enable.

When LVR enable, The H5A0XP will be reset while the operating voltage is too low (typical 2.4V).
Note: Set LVR on or off one time in your application, do not switch this bit (BIT-3).

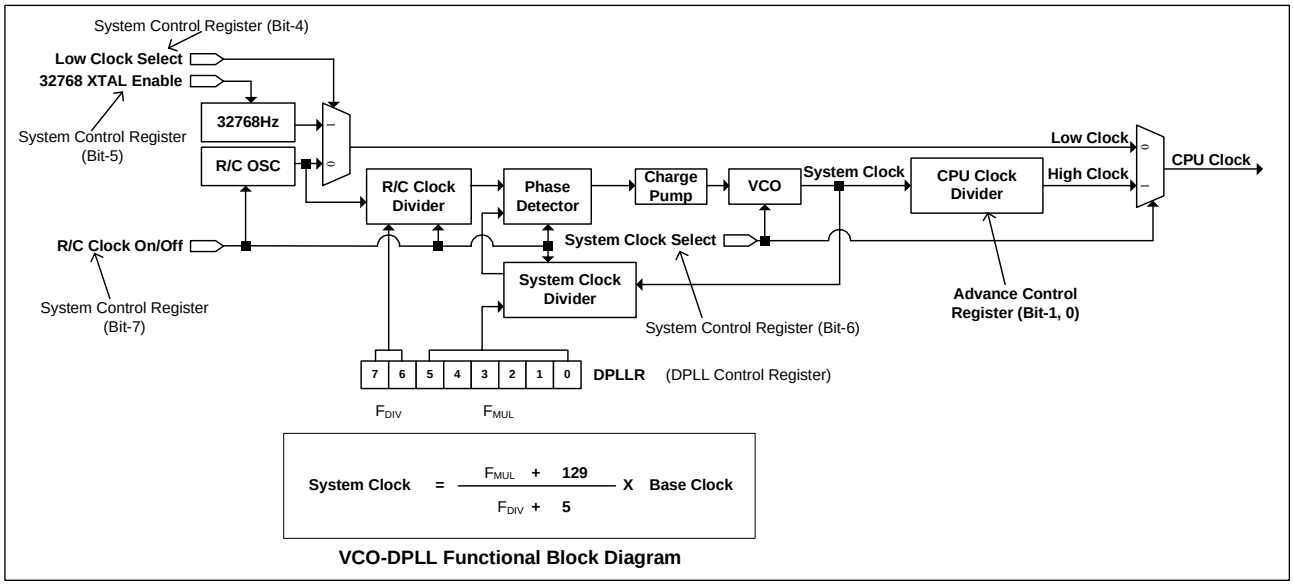
001AH,001BH,001CH,001DH:PTR Access Register(PTRAR)

001AH ,001BH,001CH,001DH, PTR Access Register(PTRAR)																
Bit No.	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	**001AH High Byte**							**001BH Mid Byte**								
Read/Write	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Reset	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit No.	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	**001CH Low Byte**							**001DH DATA**								
Read/Write	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Reset	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

The CPU can use the 24 bits register (PTR, 1AH~1CH) to access the memory data by read or write PTR_DATA(1DH), and the 24 bits PTR increases automatically after access the PTR_DATA.

001EH: DPLL Control Register(DPLLR)

001EH , DPLL Control Register(DPLLR)								
Bit No.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	control clock division		control the clock multiplier					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	1	0	1	1

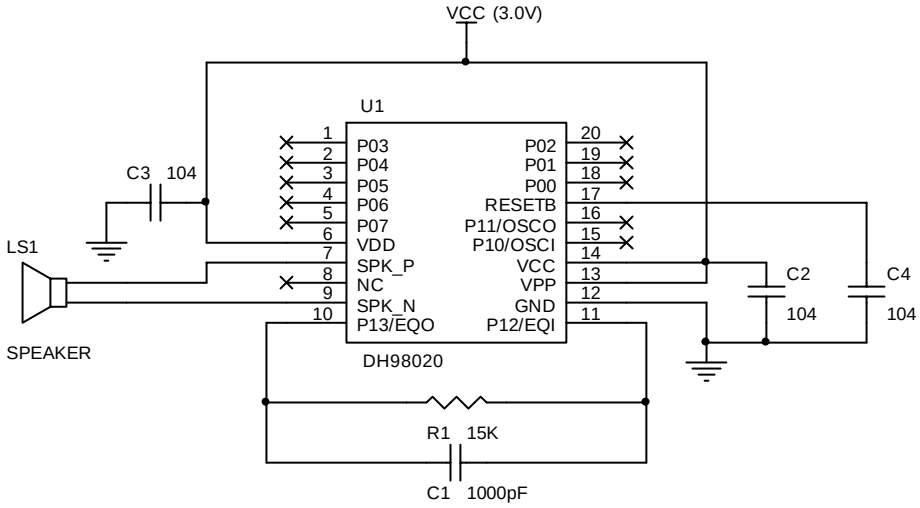


VCO-DPLL Functional Block Diagram

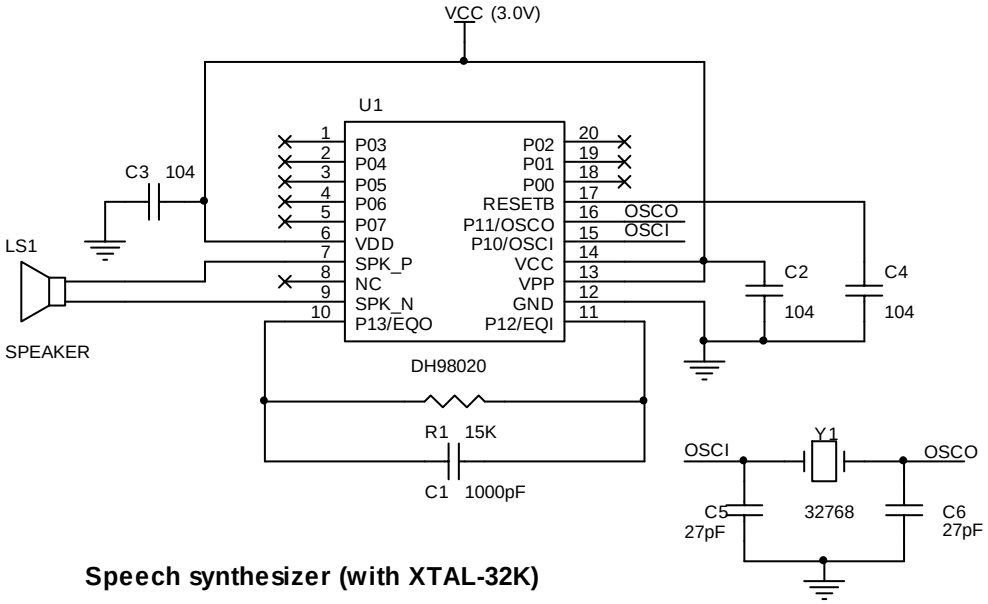
D[5:0] Control the clock multiplier(n).
D[7:6] Control clock division (m).

DPLL clock: also called High clock.
RC clock: also called Base clock.
High clock = Base Clock * (n + 129) / (m + 5).
Default after system reset: 10001011B (8BH) , High clock= 20 x Base Clock.
Typically: Base Clock = 1.85M Hz, VCC = 3.3V.
After reset, High Clock = 20.00 x 1.85M Hz = 36.00M Hz.

Application Circuit (For reference)

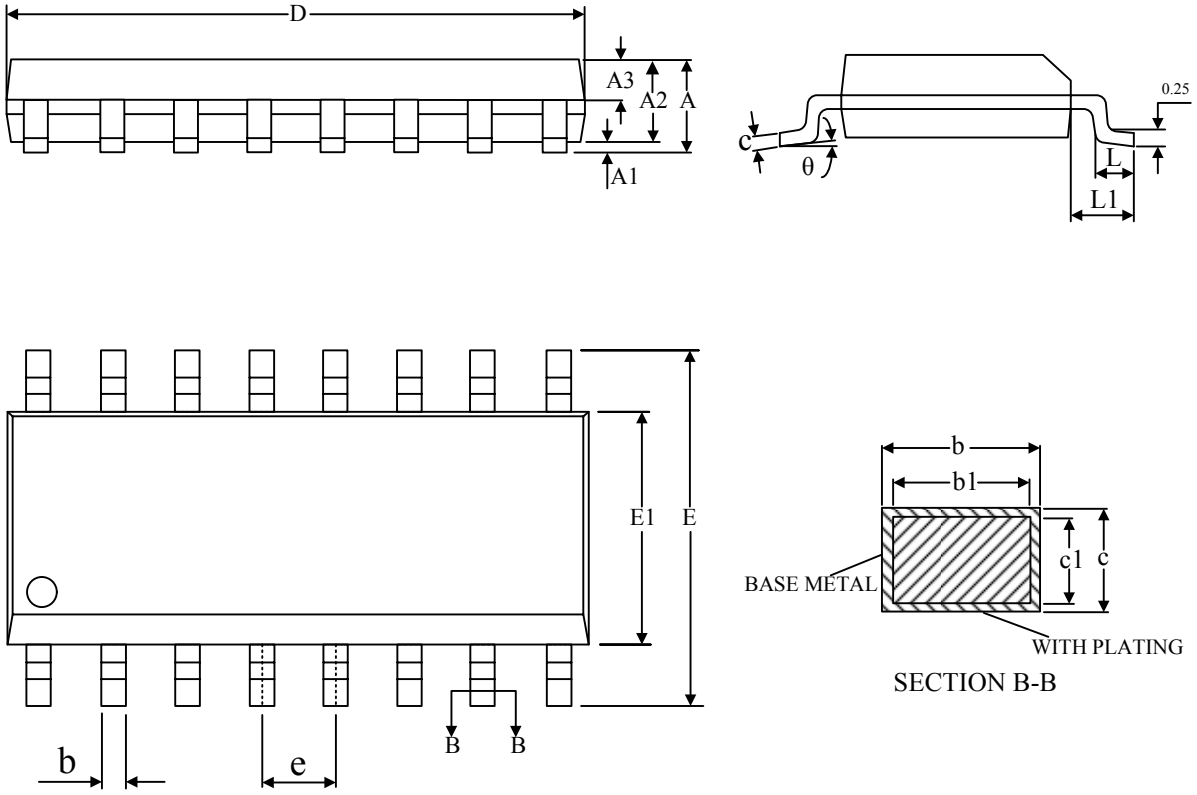


Speech synthesizer application



Speech synthesizer (with XTAL-32K)

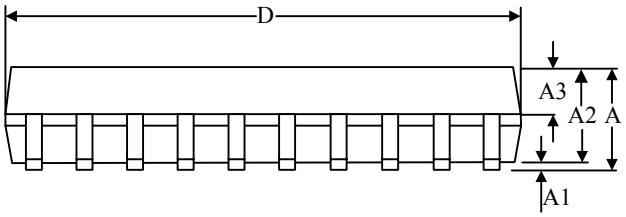
Package Drawings	16-Lead Small Outline Package (SOP) **SOP 16 (150 mil)**

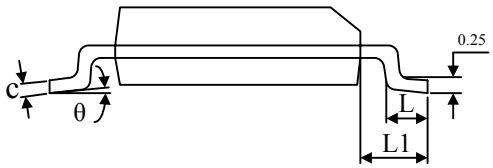


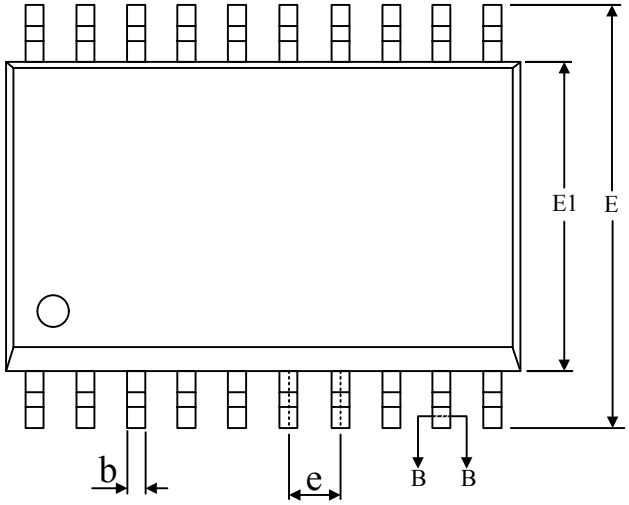
SYBBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.77	-	-	70
A1	0.08	0.18	0.28	3	7	11
A2	1.20	1.40	1.60	47	55	63
A3	0.55	0.65	0.75	22	26	30
b	0.39	-	0.48	15	-	19
b1	0.38	0.41	0.43	15	16	17
c	0.21	-	0.26	8		10
c1	0.19	0.20	0.21	7.5	7.9	8.3
D	9.70	9.90	10.10	382	390	398
E	5.80	6.00	6.20	228	236	244
E1	3.70	3.90	4.10	146	154	161
e	1.27 BSC			50 BSC		
L	0.50	0.65	0.80	20	26	31
L1	1.05 BSC			41 BSC		
θ	0	-	8°	0	-	8°

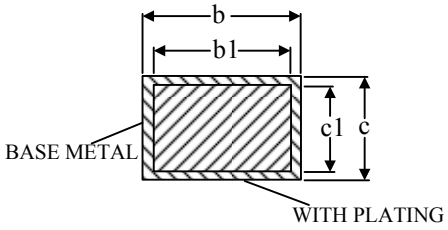
NOTE:
1. REFER TO HTFS0160225
2. CONTROLLING DIMENSION: MILLIMENTER.

Package Drawings	20-Lead Small Outline Package (SOP) **SOP 20 (300 mil)**









SECTION B-B

SYBBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	2.70	-	-	106
A1	0.10	0.20	0.30	4	8	12
A2	2.10	2.30	2.50	83	91	98
A3	0.92	1.02	1.12	36	40	44
b	0.35	-	0.44	14	-	17
b1	0.34	0.37	0.39	13.4	14.6	15.4
c	0.26	-	0.31	10		12
c1	0.24	0.25	0.26	9.4	9.8	10.2
D	12.60	12.80	13.00	496	503	512
E	10.10	10.30	10.50	398	406	413
E1	7.30	7.50	7.70	287	295	303
e	1.27 BSC			50 BSC		
L	0.70	0.85	1.00	28	33	39
L1	1.40 BSC			55 BSC		
θ	0	-	8°	0	-	8°

NOTE:
1. REFER TO HTFS0200375
2. CONTROLLING DIMENSION: MILLIMENTER.